

## 160 Output Segment/Common LCD Driver

### Description

The EK7004 is a 160 output segment/common LCD Driver adaptable to drive a large scale dot matrix panel. It uses the Thin Chip Technology(TCP) to greatly reduce the size of the LCD module. EK7004 consumes very little power. Large LCD panels can be assembled by cascading EK7004s. In Segment Mode, the input data can be either 4-bit parallel or 8-bit parallel, selected by the Mode Select pin (MD).

### Features

- CMOS process
- Logic power supply : 2.5V to 5.5V
- Low power consumption
- TCP package
- 160 LCD display output
- Supply voltage for LCD driver :15 to 40V
- Package : 196 pin TCP(Tape Carrier Package)

### Features in Segment mode

- Shift clock frequency : 14MHz at 5V
- 4bit/8bit parallel input
- Automatic transfer of enable signal
- Automatic counting in the chip select mode. The internal clock stops by automatically counting 160 of input data.

### Features in Common mode

- Shift clock frequency : 4MHz (MAX)
- Built-in 160-bit bidirectional shift register
- Single mode (160-bit shift register) or Dual Mode (two 80-bit shift registers) with these options:
  1. Y1 → Y160 Single mode
  2. Y160 → Y1 Single mode
  3. Y1 → Y80, Y81 → Y160 Dual mode
  4. Y160 → Y81, Y80 → Y1 Dual mode

### Block Diagram

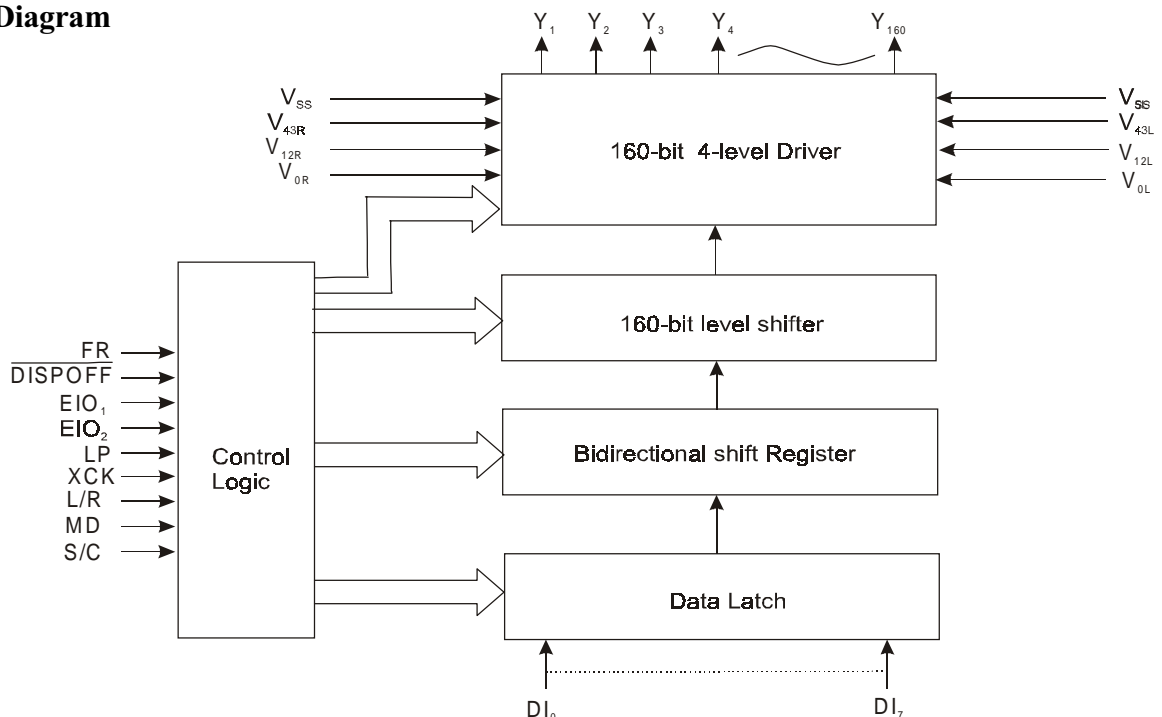


Fig.1  
1

## Pin Configuration

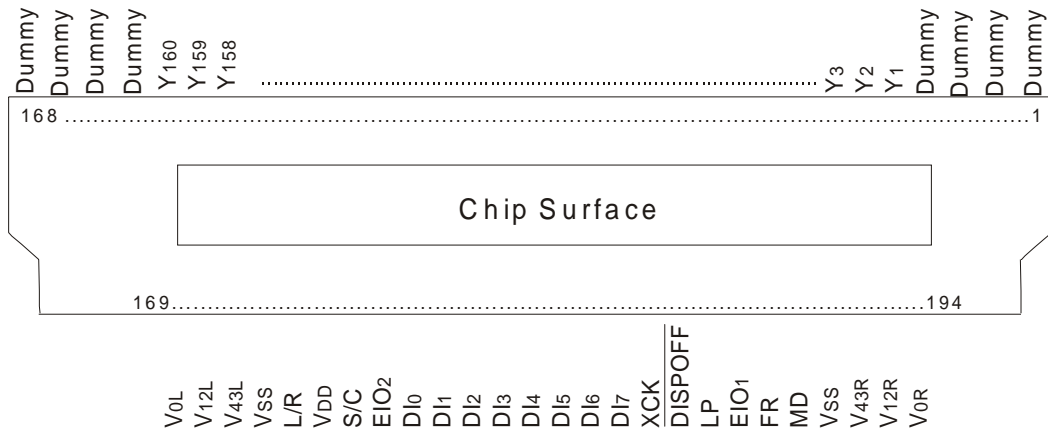


Fig.2

**Pin Designations**

<b>Pin No.</b>	<b>Symbol</b>	<b>I/O</b>	<b>Designation</b>
5 to 164	Y1-Y160	O	LCD output
169, 194	V0L, V0R	-	Power supply for LCD driver level
170, 193	V12L, V12R	-	Power supply for LCD driver level
171, 192	V43L, V43R	-	Power supply for LCD driver level
173	L/R	I	Display data shift direction selection
174	VDD	-	Power supply for logic circuit(+2.5 to +5.5V)
175	S/C	I	Segment mode/common mode selection
176	EIO <sub>2</sub>	I/O	Input/output for chip select or data of shift register
177 to 183	DI <sub>0</sub> -DI <sub>6</sub>	I	Input of display data in segment mode
184	DI <sub>7</sub>	I	Input of display data in Segment mode, or Dual mode data input in common mode
185	XCK	I	Display data shift clock input in segment mode
186	$\overline{\text{DISPOFF}}$	I	control pin input to deselect output level
187	LP	I	Latch pulse input/shift clock input for shift register in common mode
188	EIO <sub>1</sub>	I/O	Input/output for chip select or data of shift register
189	FR	I	AC-converting signal input for LCD driver waveform
190	MD	I	Mode selection
172, 191	VSS	-	Ground
1~ 4, 165~168	Dummy	-	Dummy PADS

Tab.1

## Input/Output Circuit

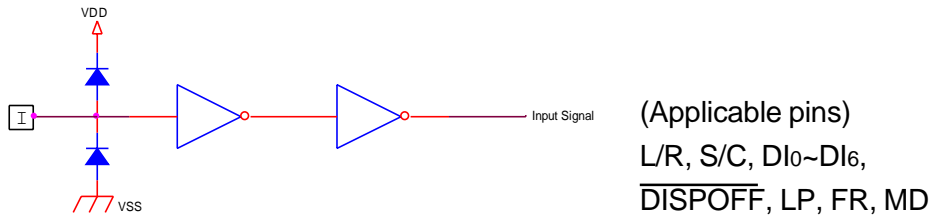


Fig.3 Input Circuit(1)

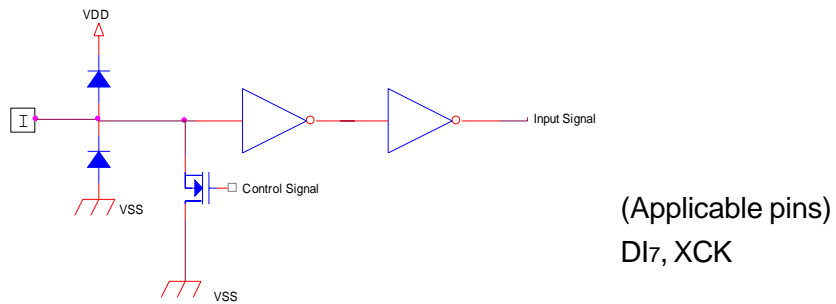


Fig.4 Input Circuit(2)

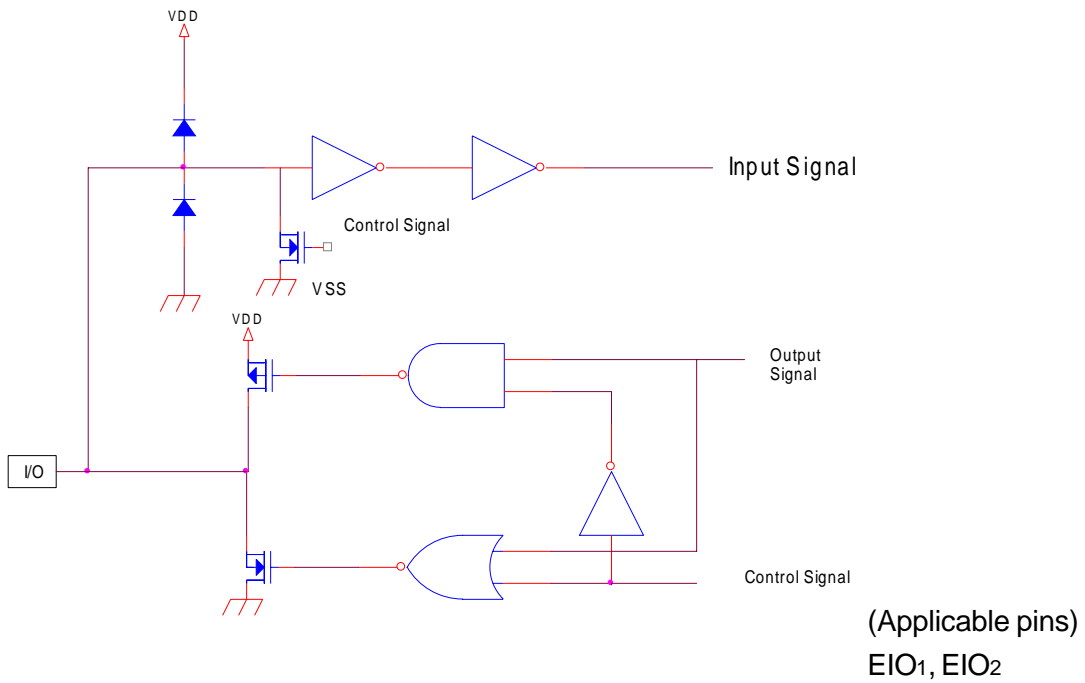


Fig.5 Input/Output Circuit

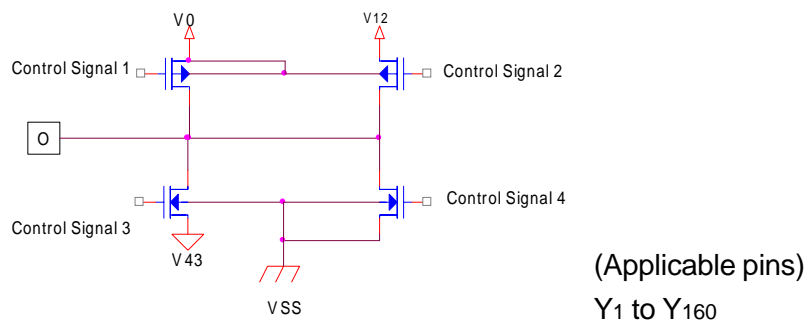


Fig.6 LCD Driver Output Circuit

## Pin Functions (Segment mode)

Symbol	Function
$V_{DD}$	Logic circuit power supply +2.5 to +5.5 V
$V_{SS}$	Ground pin
$V_{0R}, V_{0L}$ $V_{12R}, V_{12L}$ $V_{43R}, V_{43L}$	Power supply for LCD driver voltage level <ul style="list-style-type: none"> <li>● Normally, the bias voltage used is set by a resistor divider.</li> <li>● Ensure that voltages are set such that <math>V_{SS} &lt; V_{43} &lt; V_{12} &lt; V_0</math>.</li> <li>● To further reduce the difference between the output waveforms of LCD. driver output pins <math>Y_1</math> and <math>Y_{160}</math> should be externally connected to <math>V_{iR}</math> and <math>V_{iL}</math> (<math>i=0, 12, 43</math>).</li> </ul>
DI0~DI7	Input for display data <ul style="list-style-type: none"> <li>● In 4-bit parallel input mode, input data into the 4 pins DI0~DI3. Connect DI4~DI7 to <math>V_{SS}</math> or <math>V_{DD}</math>.</li> <li>● In 8-bit parallel input mode. input data into the 8 pins DI0~DI7.</li> </ul>
XCK	Input clock pin for displaying data <ul style="list-style-type: none"> <li>● Data is read on the falling edge of the clock pulse.</li> </ul>
LP	Latch pulse input for displaying data <ul style="list-style-type: none"> <li>● Data is latched on the falling edge of the clock pulse.</li> </ul>
L/R	Direction selection for reading display data <ul style="list-style-type: none"> <li>● When set to <math>V_{SS}</math>, data is read sequentially from <math>Y_{160}</math> to <math>Y_1</math>.</li> <li>● When set to <math>V_{DD}</math>, data is read sequentially from <math>Y_1</math> to <math>Y_{160}</math>.</li> </ul>
$\overline{DISPOFF}$	Control input to deselect output level <ul style="list-style-type: none"> <li>● The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit.</li> <li>● When set to <math>V_{SS}</math> level "L", the LCD driver output pins (<math>Y_1</math>~<math>Y_{160}</math>) are set to level <math>V_{SS}</math>.</li> <li>● While set to "L", the contents of the line latch are cleared, but read the display data in the data latch regardless of condition of <math>\overline{DISPOFF}</math>. When the <math>\overline{DISPOFF}</math> function is cancelled, the driver outputs deselect level (<math>V_{12}</math> or <math>V_{43}</math>), then outputs the contents of the data latch on the next falling edge of the LP. At that time, if <math>\overline{DISPOFF}</math> removal time does not meet the conditions shown in conditions, it can not output the reading data correctly.</li> </ul>
FR	AC signal for LCD driver output level <ul style="list-style-type: none"> <li>● The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit.</li> <li>● Normally, inputs a frame inversion signal.</li> <li>● The LCD driver output pin's output voltage level can be set using the line latch output signal and the FR signal.</li> <li>● Truth table is shown on page10.</li> </ul>

## Pin Functions

### (Segment mode)

Symbol	Function
MD	Mode selection <ul style="list-style-type: none"><li>● When set to <math>V_{SS}</math> level "L", 4-bit parallel input mode is selected.</li><li>● When set to <math>V_{DD}</math> level "H", 8-bit parallel input mode is selected.</li></ul> The relationship between the display data and driver output pins is shown on page11.12.13.
S/C	Segment mode/common mode selection pin <ul style="list-style-type: none"><li>● When set to <math>V_{DD}</math>, segment input mode is set.</li></ul>
EIO1 EIO2	Input/Output for chip selection <ul style="list-style-type: none"><li>● When L/R input is at <math>V_{SS}</math> level "L", EIO<sub>1</sub> is set for output, and EIO<sub>2</sub> is set for input.</li><li>● When L/R input is at <math>V_{DD}</math> level "H", EIO<sub>1</sub> is set for input, and EIO<sub>2</sub> is set for output.</li><li>● During output, set to "H" while LP*XCK is "H" After 160-bit data have been read, set to "L" for one cycle (from falling edge of XCK), after which it returns to "H".</li><li>● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 160-bits of data have been read, the chip is deselected.</li></ul>
Y <sub>1</sub> -Y <sub>160</sub>	LCD driver output <ul style="list-style-type: none"><li>● Corresponding directly to each bit of the data latch, one level(<math>V_0</math>, <math>V_{12}</math>, <math>V_{43}</math>, or <math>V_{SS}</math>) is selected for output.</li><li>● Truth table values is shown on page10.</li></ul>

Tab.3

## Pin Functions (Common mode)

Symbol	Function
$V_{DD}$	Logic circuit power supply pin connects to +2.5 to +5.5 V.
$V_{SS}$	Ground pin .
$V_{0R}, V_{0L}$ $V_{12R}, V_{12L}$ $V_{43R}, V_{43L}$	Power supply pin for LCD driver voltage bias <ul style="list-style-type: none"> <li>● Normally, the bias voltage used is set by a resistor divider.</li> <li>● Ensure that voltages are set such that <math>V_{SS} &lt; V_{43} &lt; V_{12} &lt; V_0</math>.</li> <li>● To further reduce the difference between the output waveforms of LCD driver output pins <math>Y_1</math> and <math>Y_{160}</math>, externally connect <math>V_{iR}</math> and <math>V_{iL}</math> (<math>i=0, 12, 43</math>).</li> </ul>
$EIO_1$	Bidirectional shift register input/output. <ul style="list-style-type: none"> <li>● Output when L/R is set at <math>V_{SS}</math> level "L", input when L/R is at <math>V_{DD}</math> level "H".</li> <li>● When <math>EIO_1</math> is used as input pin, it will be pull-down.</li> <li>● When <math>EIO_1</math> is used as output pin, it will not be pull-down.</li> </ul>
$EIO_2$	Bidirectional shift register input/output. <ul style="list-style-type: none"> <li>● Input when L/R is set at <math>V_{SS}</math> level "L". output when L/R is at <math>V_{DD}</math> .</li> <li>● When <math>EIO_2</math> is used as input, it will be pulled-down..</li> <li>● When <math>EIO_2</math> is used as output, it will not be pulled-down.</li> </ul>
LP	Bidirectional shift register clock pulse input <ul style="list-style-type: none"> <li>● Data is shifted on the falling edge of the clock pulse.</li> </ul>
L/R	Bidirectional shift register shift direction selection <ul style="list-style-type: none"> <li>● When set to <math>V_{SS}</math> data is shifted from <math>Y_{160}</math> to <math>Y_1</math>.</li> <li>● When set to <math>V_{DD}</math>, data is shifted from <math>Y_1</math> to <math>Y_{160}</math>.</li> </ul>
$\overline{DISPOFF}$	Control input pin to deselect output level <ul style="list-style-type: none"> <li>● The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit.</li> <li>● When set to "L", the LCD driver output pins (<math>Y_1</math>-<math>Y_{160}</math>) are set to level <math>V_{SS}</math>.</li> <li>● While set to "L", the contents of the shift register are cleared. When the <math>\overline{DISPOFF}</math> function is cancelled, the driver outputs deselect level (<math>V_{12}</math> or <math>V_{43}</math>), and the shift data is read on the falling edge of the LP. At that time, if the <math>\overline{DISPOFF}</math> removal time does not meet the conditions shown in Page 22, then the shift data is not read correctly.</li> </ul>
FR	AC signal input for LCD driver output level <ul style="list-style-type: none"> <li>● The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit.</li> <li>● The LCD driver output voltage level can be set by using the shift register output signal and the FR signal.</li> <li>● Truth table is shown on page10.</li> </ul>

Tab.4

## Pin Functions (Common mode)

Symbol	Function
MD	Mode selection ● When set to V <sub>SS</sub> level "L", Single Mode operation is selected, when set to V <sub>DD</sub> level "H", Dual Mode operation is selected.
DI <sub>7</sub>	Dual Mode data input ● According to the data shift direction of the data shift register, data can be input starting from the 81st bit. ● When the chip is used as Dual Mode, DI <sub>7</sub> will be pulled-down. ● When the chip is used as Single Mode, DI <sub>7</sub> will not be pulled-down.
S/C	Segment mode/common mode selection ● When set to V <sub>SS</sub> level "L", Common Mode is set.
DI <sub>0</sub> ~DI <sub>6</sub>	Not used ● Connect DI <sub>0</sub> ~DI <sub>6</sub> to V <sub>SS</sub> or V <sub>DD</sub> . Avoiding floating.
XCK	Not used ● XCK is pull-down in common mode, so connect them to V <sub>SS</sub> or open.
Y <sub>1</sub> ~Y <sub>160</sub>	LC driver output ● Corresponding directly to each bit of the shift register, one level (V <sub>0</sub> , V <sub>12</sub> , V <sub>43</sub> , or V <sub>SS</sub> ) is selected. ● Truth table is shown on page10.

Tab.5

## Functional Operations

### Truth Table

#### (Segment Mode)

FR	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output Voltage Level( $Y_1$ - $Y_{160}$ )
L	L	H	$V_{43}$
L	H	H	$V_{SS}$
H	L	H	$V_{12}$
H	H	H	$V_{SS}$
X	X	L	$V_{SS}$

Here,  $V_{SS} < V_{43} < V_{12} < V_0$ , H: $V_{DD}$  (+2.5 to +5.5V), L: $V_{SS}$ (0 V)

X:Don't care

Tab.6

#### (Common Mode)

FR	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output Voltage Level( $Y_1$ - $Y_{160}$ )
L	L	H	$V_{43}$
L	H	H	$V_0$
H	L	H	$V_{12}$
H	H	H	$V_{SS}$
X	X	L	$V_{SS}$

Here,  $V_{SS} < V_{43} < V_{12} < V_0$ , H: $V_{DD}$  (+2.5 to +5.5V), L: $V_{SS}$ (0 V)

X:Don't care

Tab.7

Note: There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD driver

Supply proper voltage according to each power pin specification.

That time "Don't care" should be connected to "H" or "L". Do not leave them open.

## Relationship between the Display Data and Driver Output pins

(Segment Mode)

(a)4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Figure of Clock						
					40 clock	39 clock	38 clock	.....	3 clock	2 clock	1 clock
L	L	Output	Input	DI0	Y1	Y5	Y9	.....	Y149	Y153	Y157
				DI1	Y2	Y6	Y10	.....	Y150	Y154	Y158
				DI2	Y3	Y7	Y11	.....	Y151	Y155	Y159
				DI3	Y4	Y8	Y12	.....	Y152	Y156	Y160
L	H	Input	Output	DI0	Y160	Y156	Y152	.....	Y12	Y8	Y4
				DI1	Y159	Y155	Y151	.....	Y11	Y7	Y3
				DI2	Y158	Y154	Y150	.....	Y10	Y6	Y2
				DI3	Y157	Y153	Y149	.....	Y9	Y5	Y1

Tab.8

(b)8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Figure of Clock						
					20 clock	19 clock	18 clock	.....	3 clock	2 clock	1 clock
H	L	Output	Input	DI0	Y1	Y9	Y17	.....	Y137	Y145	Y153
				DI1	Y2	Y10	Y18	.....	Y138	Y146	Y154
				DI2	Y3	Y11	Y19	.....	Y139	Y147	Y155
				DI3	Y4	Y12	Y20	.....	Y140	Y148	Y156
				DI4	Y5	Y13	Y21	.....	Y141	Y149	Y157
				DI5	Y6	Y14	Y22	.....	Y142	Y150	Y158
				DI6	Y7	Y15	Y23	.....	Y143	Y151	Y159
				DI7	Y8	Y16	Y24	.....	Y144	Y152	Y160
H	H	Input	Output	DI0	Y160	Y152	Y144	.....	Y24	Y16	Y8
				DI1	Y159	Y151	Y143	.....	Y23	Y15	Y7
				DI2	Y158	Y150	Y142	.....	Y22	Y14	Y6
				DI3	Y157	Y149	Y141	.....	Y21	Y13	Y5
				DI4	Y156	Y148	Y140	.....	Y20	Y12	Y4
				DI5	Y155	Y147	Y139	.....	Y19	Y11	Y3
				DI6	Y154	Y146	Y138	.....	Y18	Y10	Y2
				DI7	Y153	Y145	Y137	.....	Y17	Y9	Y1

Tab.9

**(Common Mode)**

MD	L/R	Data Transfer Direction	EIO1	EIO2	DI7
L (Single)	L(shift to left)	$Y_{160} \rightarrow Y_1$	Output	Input	x
	H(shift to right)	$Y_1 \rightarrow Y_{160}$	Input	Output	x
H (Dual)	L(shift to left)	$Y_{160} \rightarrow Y_{81}$ $Y_{80} \rightarrow Y_1$	Output	Input	Input
	H(shift to right)	$Y_1 \rightarrow Y_{80}$ $Y_{81} \rightarrow Y_{160}$	Input	Output	Input

Tab.10

L:  $V_{SS}$ (0 V), H:  $V_{DD}$  (+2.5V to +5.5V), x: Don't Care

Note: "Don't care" should be connected to "H" or "L". Do not leave them open

## Connection Examples of Plural Segment Drives

(a) Case of L/R="L"

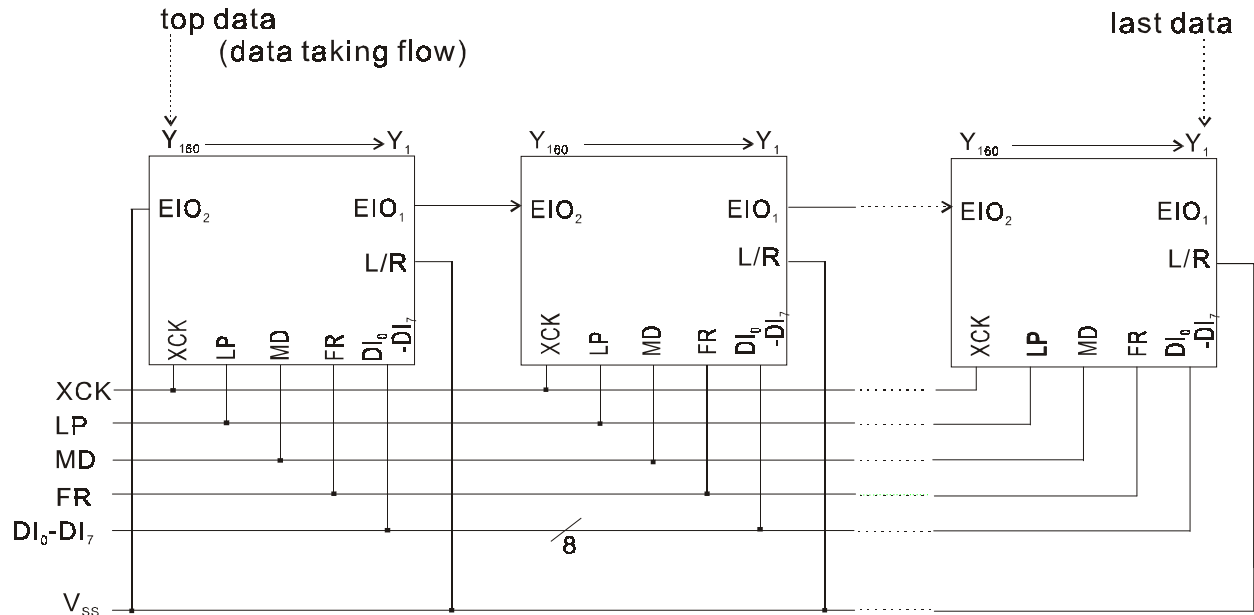


Fig.7

(b) Case of L/R="H"

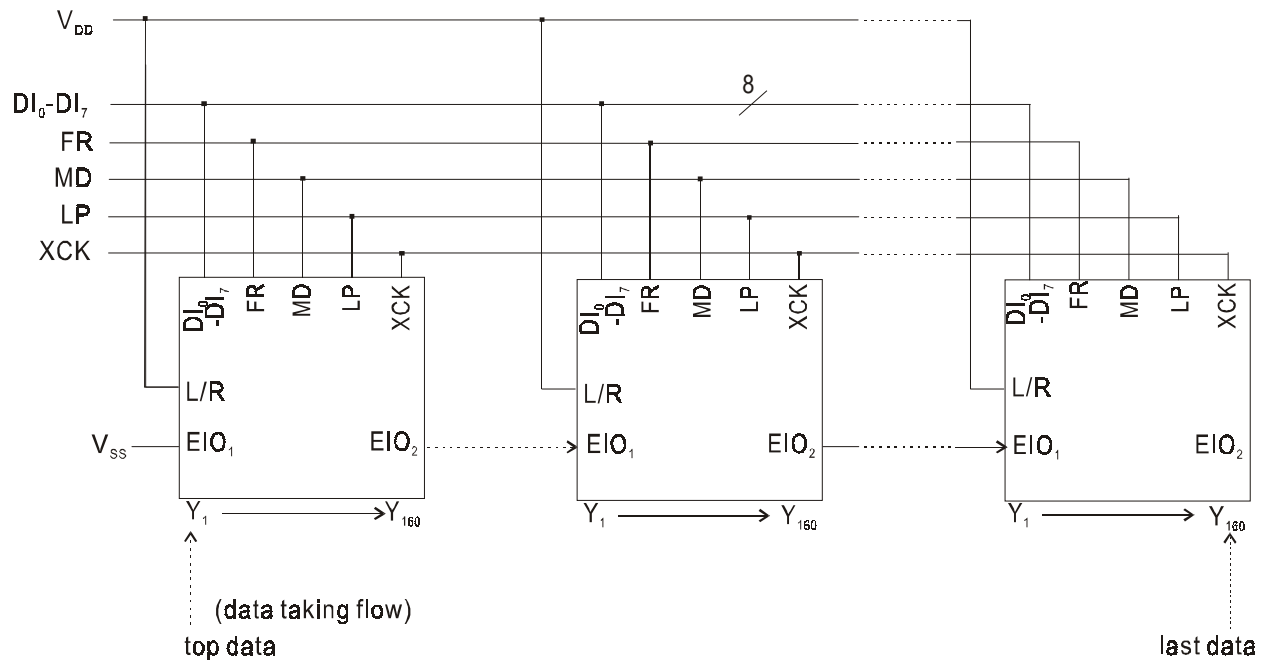


Fig.8

## Timing Chart of 4-Device cascade Connection of Segment Drivers

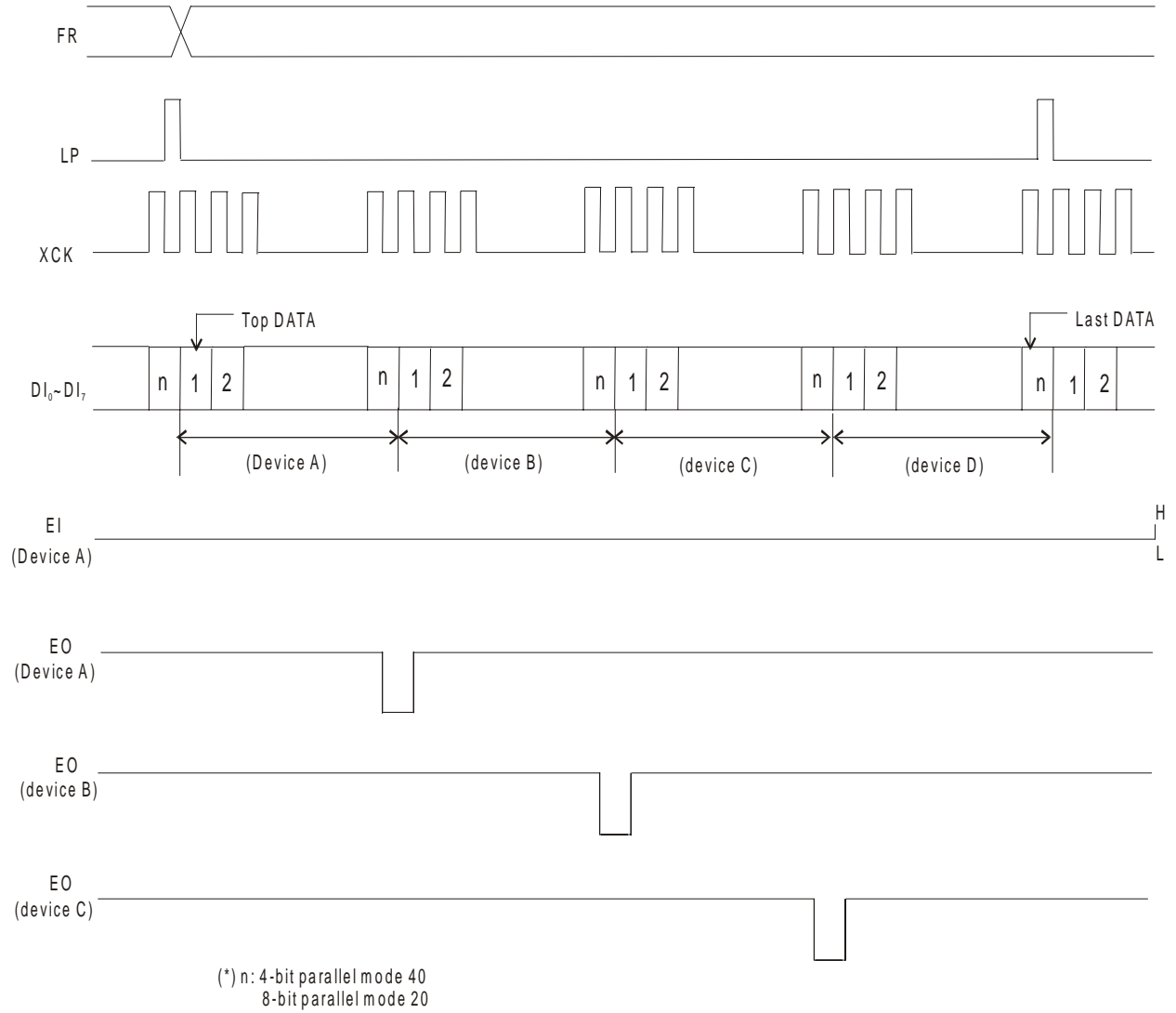


Fig.9

## Connection Examples for Plural Common Drivers

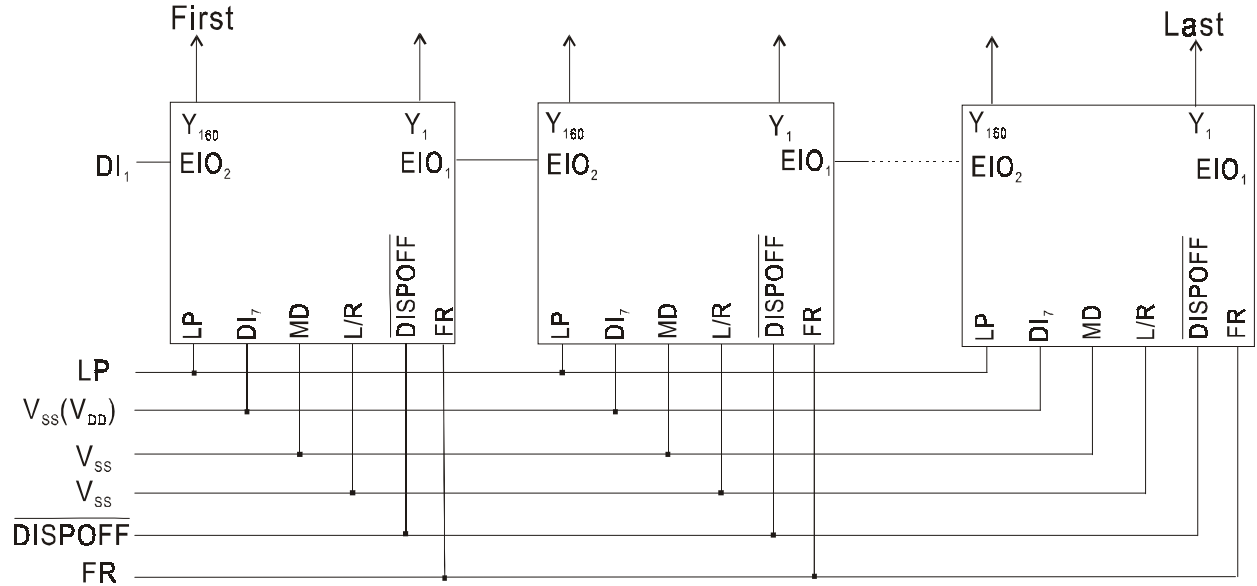


Fig.10 Single Mode (Shifting toward left)

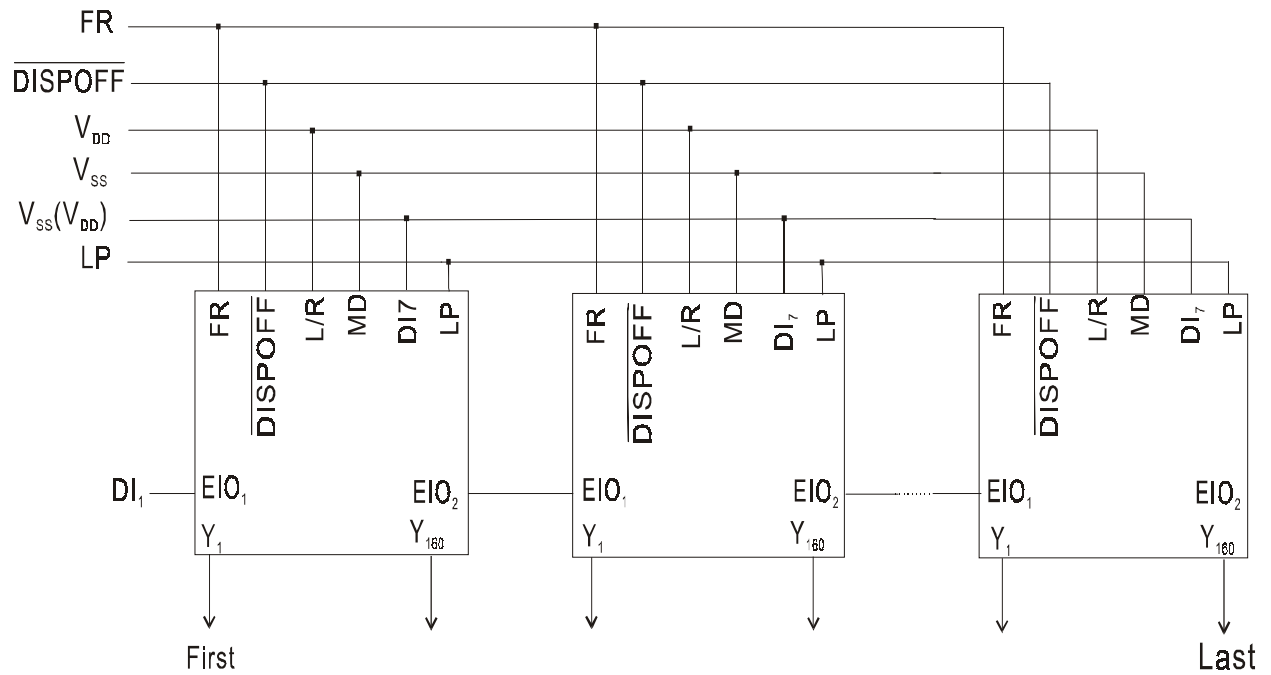


Fig.11 Single Mode (Shifting toward right)

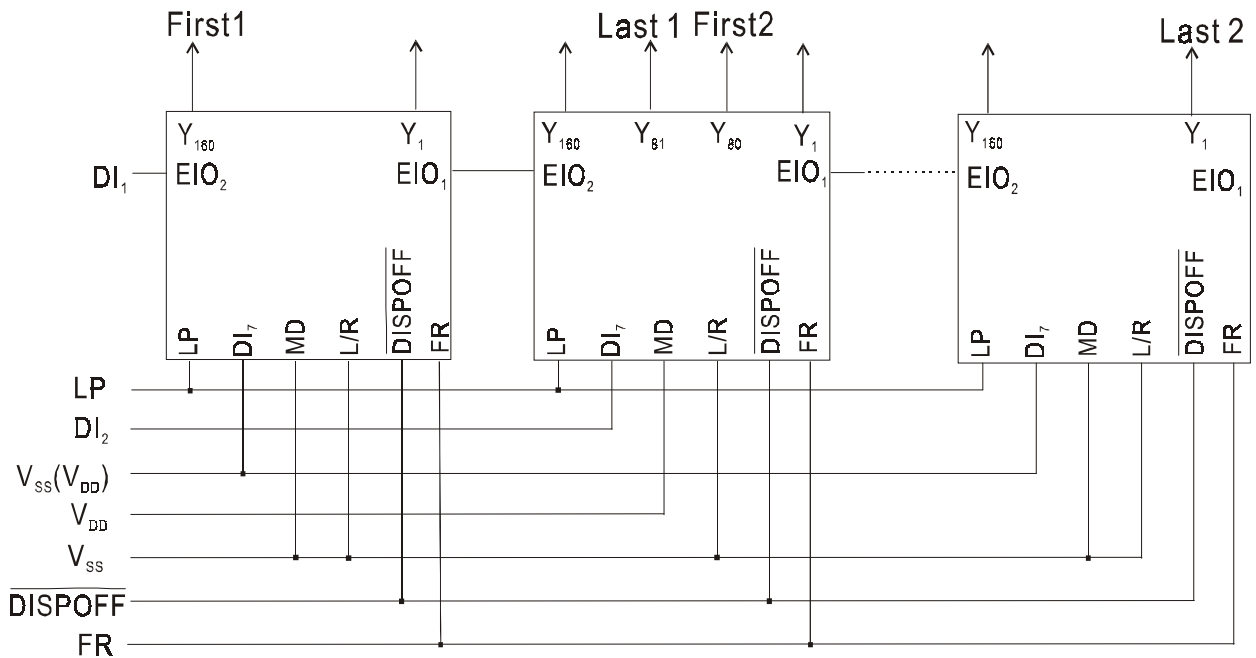


Fig.12 Dual Mode (Shifting toward left)

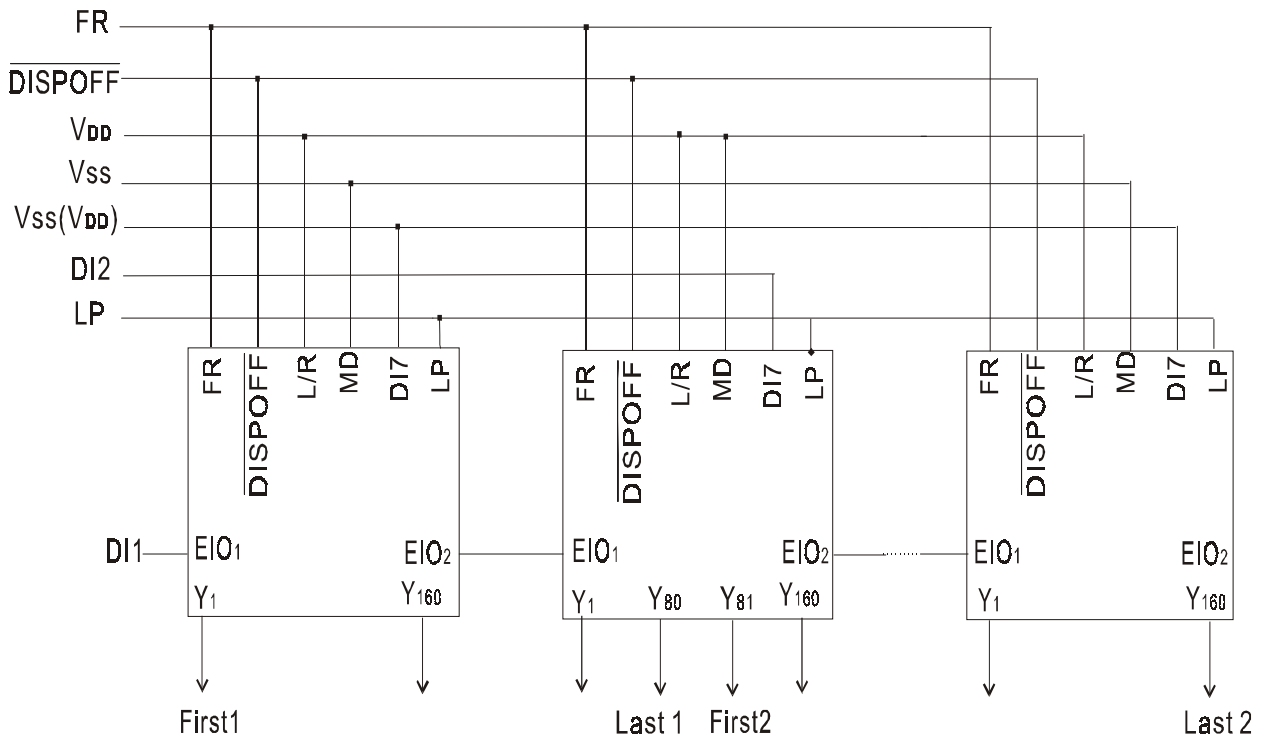


Fig.13 Dual Mode (Shifting toward right)

### Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply voltage(1)	$V_{DD}$	Ta=25°C Referenced to $V_{SS}$ (0 V)	$V_{DD}$	-0.3 to +7.0	V
Supply voltage(2)	$V_0$		$V_{0L}, V_{0R}$	-0.3 to +45.0	V
	$V_{12}$		$V_{12L}, V_{12R}$	-0.3 to $V_0+0.3$	V
	$V_{43}$		$V_{43L}, V_{43R}$	-0.3 to $V_0+0.3$	V
Input voltage	$V_1$		DI <sub>0-7</sub> , XCK, LP, L/P, FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , $\overline{DISPOFF}$	-0.3 to $V_{DD}+0.3$	V
Storage temperature	Tstg			-45 to +125	°C

Tab.11

### Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage(1)	$V_{DD}$	Referenced to $V_{SS}$ (0 V)	$V_{DD}$	+2.5		+5.5	V
Supply voltage(2)	$V_0$		$V_{0L}, V_{0R}$	+15.0		+40	V
Storage temperature	$T_{opr}$			-20		+85	°C

Tab.12

Note: Ensure that voltages are set such that  $V_{SS} < V_{43} < V_{12} < V_0$

## Electrical Characteristics

### DC Characteristics

(Segment Mode)

( $V_{SS}=0$  V,  $V_{DD}=+2.5$ V to  $+5.5$ V,  $V_0=+15.0$  to  $+40$  V,  $T_a=-20$  to  $+85$  °C )

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit	
Input voltage	$V_{IH}$		$DI_{0-7}$ , XCK, LP, L/R, FR, MD, S/C,	$0.8V_{DD}$			V	
	$V_{IL}$		EIO <sub>1</sub> , EIO <sub>2</sub> , DISPOFF			$0.2V_{DD}$	V	
Output voltage	$V_{OH}$	$I_{OH}=-0.4$ mA	EIO <sub>1</sub> ,EIO <sub>2</sub>	$V_{DD}-0.4$			V	
	$V_{OL}$	$I_{OL}=+0.4$ mA				+0.4	V	
Input leakage current	$I_{LH}$	$V_1=V_{DD}$	$DI_{0-7}$ , XCK, LP, L/R, FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , DISPOFF			+10.0	μA	
	$I_{LL}$	$V_1=V_{SS}$				-10.0	μA	
Output resistance	$R_{ON}$	$ \Delta V_{ON} =0.5$ V	$V_0=+40.0$ V $V_0=+30.0$ V $V_0=+20.0$ V	$Y_1-Y_{160}$		0.7	1.0	KΩ
						1.0	1.5	
						1.5	2.0	
Stand-by current	$I_{STB}$	*1	$V_{SS}$			50.0	μA	
Consumed current(1) (Deselection)	$I_{DD1}$	*2	$V_{DD}$			2.0	mA	
Consumed current(2) (Selection)	$I_{DD2}$	*3	$V_{DD}$			8.0	mA	
Consoumed current	$I_0$	*4	$V_0$			1.0	mA	

Tab.13

Note:

\*1  $V_{DD}=+5.0$ V,  $V_0=+40$ V,  $V_1=V_{SS}$

\*2  $V_{DD}=+5.0$ V,  $V_0=+40$ V,  $f_{XCK}=14$ MHz, No-load,  $EI=V_{DD}$

The input data is turned over by data taking clock (4-bit parallel input mode)

\*3  $V_{DD}=+5.0$ V,  $V_0=+40$ V,  $f_{XCK}=14$ MHz, No-load,  $EI=V_{SS}$

The input data is turned over by data taking clock (4-bit parallel input mode)

\*4  $V_{DD}=+5.0$ V,  $V_0=+40$ V,  $f_{XCK}=14$ MHz,  $f_{LP}=41.6$ KHz,  $f_{FR}=80$ Hz, No-load

The input data is turned over by data taking clock (4-bit parallel input mode)

(Common Mode)

( $V_{SS}=0\text{ V}$ ,  $V_{DD}=+2.5\text{V to }+5.5\text{V}$ ,  $V_0=+15.0\text{ to }+40\text{ V}$ ,  $T_a=-20\text{ to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	$V_{IH}$		$DI_{0-7}$ , XCK, LP, L/R, FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , DISPOFF	$0.8V_{DD}$			V
	$V_{IL}$					$0.2V_{DD}$	V
Output voltage	$V_{OH}$	$I_{OH}=-0.4\text{mA}$	EIO <sub>1</sub> , EIO <sub>2</sub>	$V_{DD}-0.4$			V
	$V_{OL}$	$I_{OL}=+0.4\text{mA}$				+0.4	V
Input leakage current	$I_{LH}$	$V_1=V_{DD}$	$DI_{0-6}$ , LP, L/R, FR, MD, S/C, DISPOFF			+10.0	$\mu\text{A}$
	$I_{LL}$	$V_1=V_{SS}$	$DI_{0-7}$ , XCK, LP, L/R, FR, MD, S/C, EIO <sub>1</sub> , EIO <sub>2</sub> , DISPOFF			-10.0	$\mu\text{A}$
Input pull-down current	$I_{PD}$	$V_1=V_{DD}$	XCK, EIO <sub>1</sub> , EIO <sub>2</sub> , DI <sub>7</sub>			100.0	$\mu\text{A}$
Output resistance	$R_{ON}$	$ \Delta V_{ON} =0.5\text{V}$	$V_0=+40.0\text{V}$ $V_0=+30.0\text{V}$ $V_0=+20.0\text{V}$ $Y_1\sim Y_{160}$		0.7	1.0	K $\Omega$
					1.0	1.5	
					1.5	2.0	
Stand-by current	$I_{STB}$	*1	$V_{SS}$			50.0	$\mu\text{A}$
Consumed current(1)	$I_{DD1}$	*2	$V_{DD}$			80.0	$\mu\text{A}$
Consumed current(2)	$I_{DD2}$	*3	$V_0$			160.0	$\mu\text{A}$

Tab.14

\*1  $V_{DD}=+5.0\text{V}$ ,  $V_0=+40\text{V}$ ,  $V_1=V_{SS}$

\*2  $V_{DD}=+5.0\text{V}$ ,  $V_0=+40\text{V}$ ,  $f_{LP}=41.6\text{KHz}$ ,  $f_{FR}=80\text{Hz}$ , case of 1/480 duty operation, No-load

## AC Characteristics

(Segment Mode 1)

( $V_{SS}=0\text{ V}$ ,  $V_{DD}=+4.5\text{V to }+5.5\text{V}$ ,  $V_0=+15.0\text{ to }+40\text{ V}$ ,  $T_a=-20\text{ to }+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	$t_{WCK}$	$t_r, t_f \leq 10\text{ ns}$	71			ns
Shift clock "H" pulse width	$t_{WCKH}$		23			ns
Shift clock "L" pulse width	$t_{WCKL}$		23			ns
Data setup time	$t_{DS}$		10			ns
Data Hold time	$t_{DH}$		20			ns
Latch pulse"H"pulse width	$t_{WLPH}$		23			ns
Shift clock rise to Latch pulse rise time	$t_{LD}$		0			ns
Shift clock fall to Latch pulse fall time	$t_{SL}$		25			ns
Latch pulse rise to Shift clock rise time	$t_{LS}$		25			ns
Latch pulse fall to Shift clock fall time	$t_{LH}$		25			ns
Input signal rise time*2	$t_r$				50	ns
Input signal fall time*2	$t_f$				50	ns
Enable setup time	$t_s$		21			ns
$\overline{\text{DISPOFF}}$ removal time	$t_{SD}$		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	$t_{WDL}$		1.2			$\mu\text{s}$
Output delay time(1)	$t_D$	$C_L=15\text{pF}$			40	ns
Output delay time(2)	$t_{pd1}, t_{pd2}$	$C_L=15\text{pF}$			1.2	$\mu\text{s}$
Output delay time(3)	$t_{pd3}$	$C_L=15\text{pF}$			1.2	$\mu\text{s}$

Tab.15

Note:

\*1 Take the cascade connection into consideration

\*2  $(t_{CK}-t_{WCKL}-t_{WCLK})/2$  is maximum in the case of high speed operation

(Segment Mode 2)

( $V_{SS}=0$  V,  $V_{DD}=+2.5$ V to  $+4.5$ V,  $V_0=+15.0$  to  $+40$  V,  $T_a=-20$  to  $+85$  °C )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	$t_{WCK}$	$t_r, t_f \leq 11$ ns	125			ns
Shift clock "H" pulse width	$t_{WCKH}$		51			ns
Shift clock "L" pulse width	$t_{WCKL}$		51			ns
Data setup time	$t_{DS}$		30			ns
Data Hold time	$t_{DH}$		40			ns
Latch pulse"H"pulse width	$t_{WLPH}$		51			ns
Shift clock rise to Latch pulse rise time	$t_{LD}$		0			ns
Shift clock fall to Latch pulse fall time	$t_{SL}$		51			ns
Latch pulse rise to Shift clock rise time	$t_{LS}$		51			ns
Latch pulse fall to Shift clock fall time	$t_{LH}$		51			ns
Input signal rise time*2	$t_r$				50	ns
Input signal fall time*2	$t_f$				50	ns
Enable setup time	$t_s$		36			ns
$\overline{\text{DISPOFF}}$ removal time	$t_{SD}$		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	$t_{WDL}$		1.2			$\mu$ s
Output delay time(1)	$t_D$	$C_L=15$ pF			78	ns
Output delay time(2)	$t_{pd1}, t_{pd2}$	$C_L=15$ pF			1.2	$\mu$ s
Output delay time(3)	$t_{pd3}$	$C_L=15$ pF			1.2	$\mu$ s

Tab.16

Note:

\*1 Take the cascade connection into consideration

\*2  $(t_{CK}-t_{WCKL}-t_{WCLK})/2$  is maximum in the case of high speed operation

(Timing Characteristics of Segment Mode)

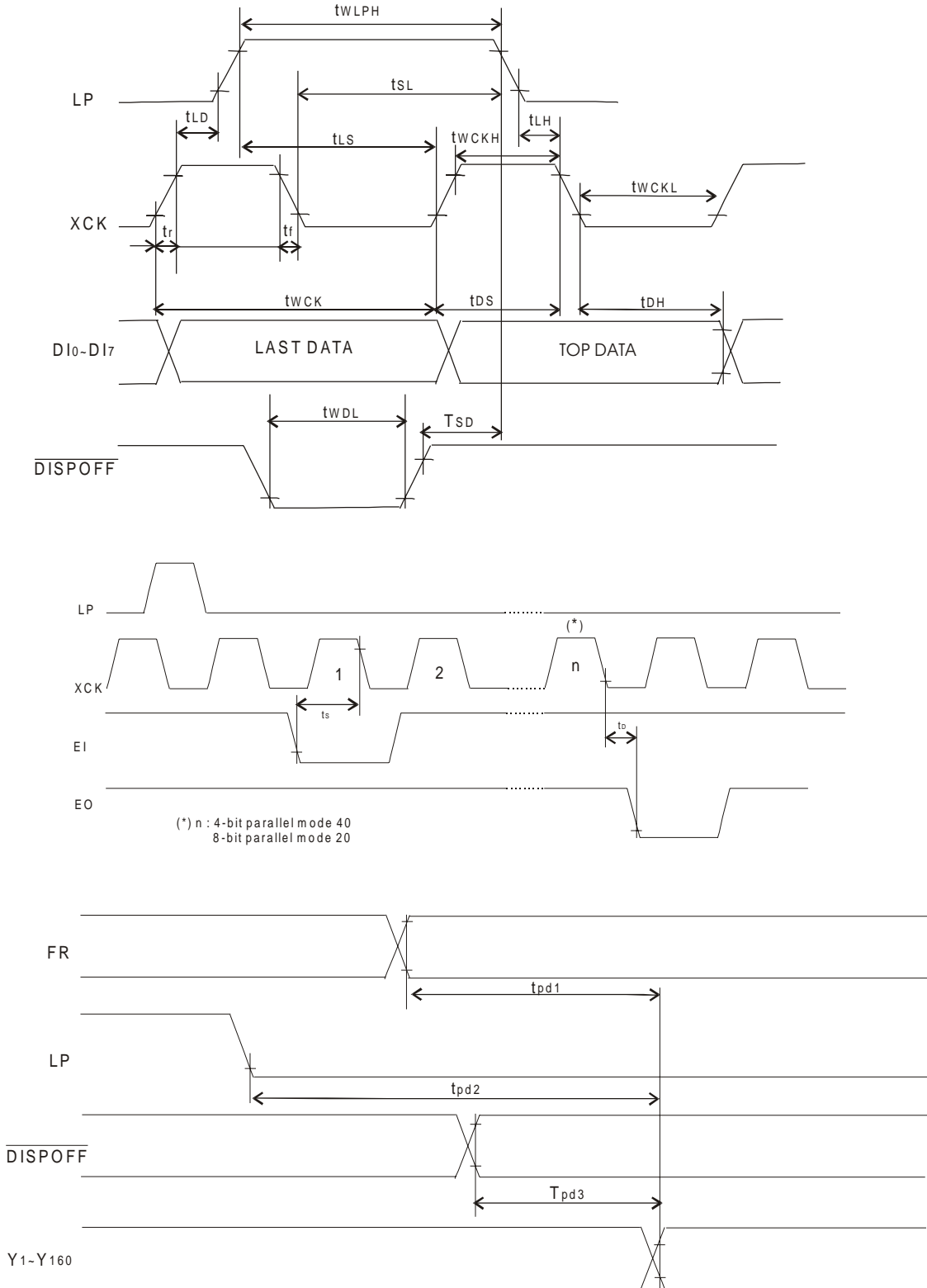


Fig.14

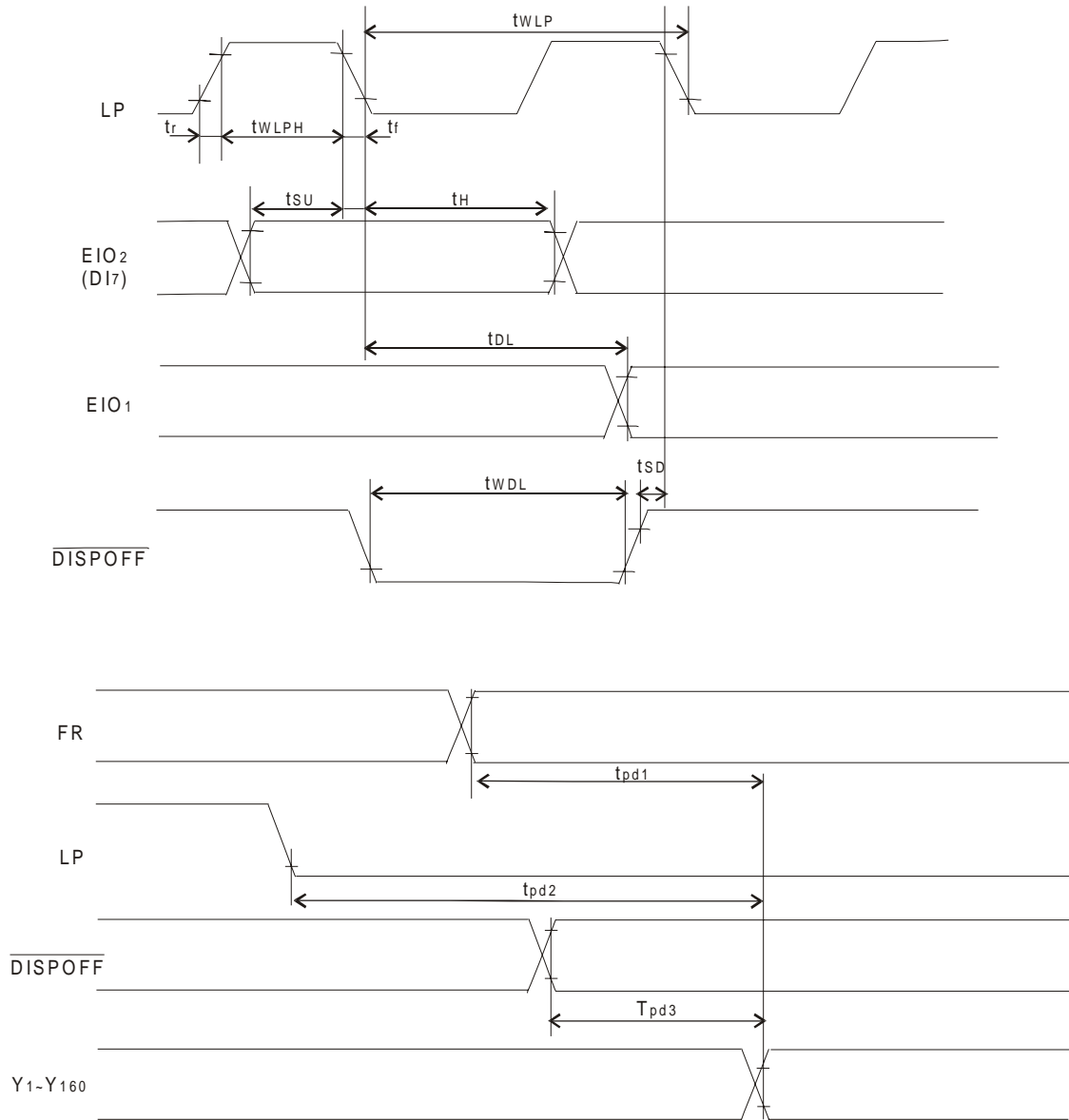
(Common Mode)

( $V_{SS}=0$  V,  $V_{DD}=+2.5$ V to +5.5V,  $V_0=+15.0$  to +40 V,  $T_a=-20$  to +85 °C )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	$t_{WLP}$	$t_r, t_f \leq 20$ ns	250			ns
Shift clock "H" pulse width	$t_{WLPH}$	$V_{DD}=+5.0$ V $\pm 10\%$	15			ns
		$V_{DD}=+2.5$ V~ +4.5V	30			
Data setup time	$t_{SU}$		30			ns
Data Hold time	$t_H$		50			ns
Input signal rise time	$t_r$				50	ns
Input signal fall time	$t_f$				50	ns
$\overline{\text{DISPOFF}}$ removal time	$t_{SD}$		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	$t_{WDL}$		1.2			$\mu$ s
Output delay time(1)	$t_{DL}$	$C_L=15$ pF			200	ns
Output delay time(2)	$t_{pd1}, t_{pd2}$	$C_L=15$ pF			1.2	$\mu$ s
Output delay time(3)	$t_{pd3}$	$C_L=15$ pF			1.2	$\mu$ s

Tab.17

(Timing Characteristics of Common Mode)



[L/R="L"]

Fig.15

## Example of system Configuration

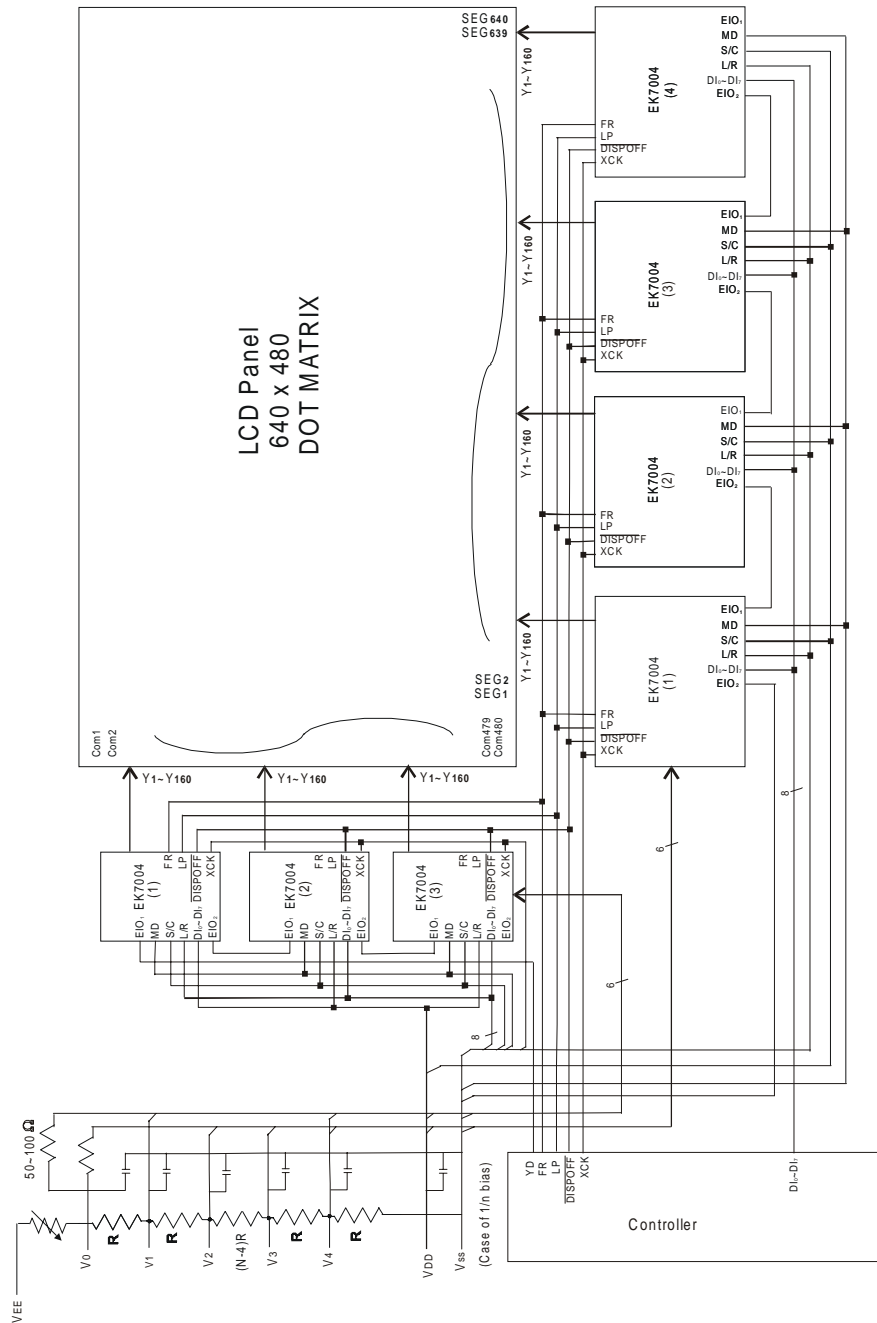


Fig.16

## **Example of Typical Characteristic**

<b>Parameter</b>	<b>Condition</b>	<b>Min.</b>	<b>Typ.</b>	<b>Max.</b>	<b>Unit</b>
Typical Fundamental Rating Propagation Delay Time	Ta=+2.5°C , Vss=0V, V <sub>DD</sub> =+5.0V		10		ns

Tab.18

## Precaution

- Precaution when connecting or disconnecting the power

This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.
- We recommend you connecting the serial resistor(50~100Ω ) or fuse to the LC drive power V<sub>0</sub> of the system as a current limiter. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on  $\overline{\text{DISPOFF}}$  function. After that, cancel the  $\overline{\text{DISPOFF}}$  function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V<sub>s</sub> on  $\overline{\text{DISPOFF}}$  function. After that, disconnect the logic system power after disconnecting the LC drive power. When connecting the power supply, show the following recommend sequence.

