240 Output Segment/Common LCD Driver

Description

The EK7005 is a 240 output segment/common LCD Driver adaptable to drive a large scale dot matrix panel. It uses the Thin Chip Technology(TCP) to greatly reduce the size of the LCD module. EK7005 consumes very little power. Large LCD panels can be assembled by cascading EK7005s. In Segment Mode, the input data can be either 4-bit parallel or 8-bit parallel, selected by the Mode Select pin (MD).

Features

- CMOS process
- Logic power supply : 2.5V to 5.5V
- Low power consumption
- TCP package
- 240 LCD display output
- Supply voltage for LCD driver :15 to 40V
- Package : 276 pin TCP(Tape Carrier Package)

Features in Segment mode

- Shift clock frequency : 14MHz at 5V
- 4bit/8bit parallel input
- Automatic transfer of enable signal
- Automatic counting in the chip select mode. The internal clock stops by automatically counting 240 of input data.

Features in Common mode

- Shift clock frequency : 4MHz (MAX)
- Built-in 240-bit bidirectional shift register
- Single mode (240-bit shift register) or Dual Mode (two 120-bit shift registers) with these options:
  1. Y1 ⟶ Y240 Single mode
  2. Y240 ⟶ Y1 Single mode
  3. Y1 ⟶ Y120, Y121 ⟶ Y240 Dual mode
  4. Y240 ⟶ Y121, Y120 ⟶ Y1 Dual mode

Block Diagram

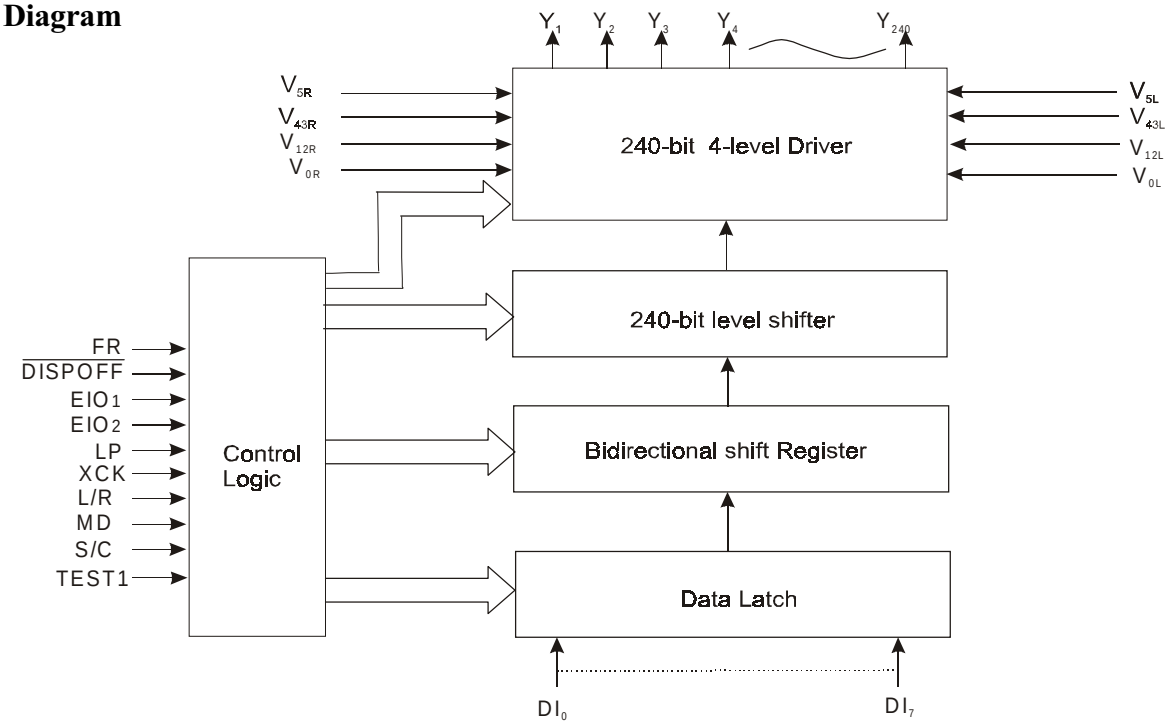


Fig.1

Pin Configuration

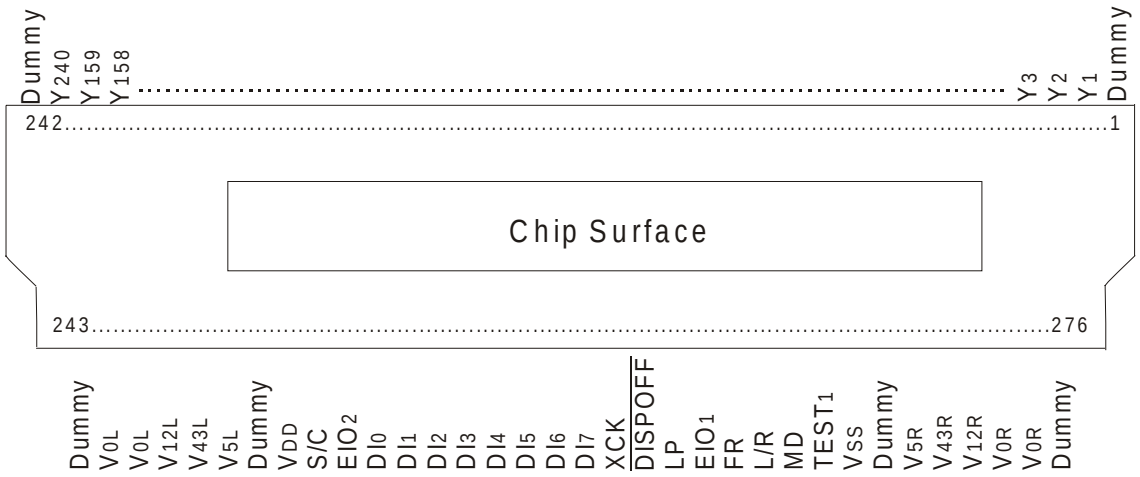


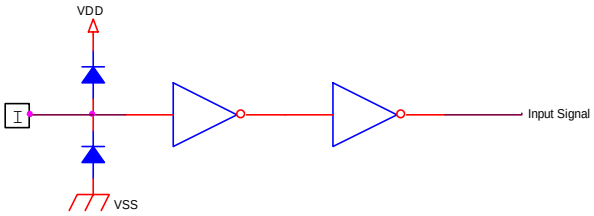
Fig.2

Pin Designations

Pin No.	Symbol	I/O	Designation
2 to 241	V_1-V_{240}	O	LCD output
244, 245, 274, 275	V_{0L}, V_{0R}	-	Power supply for LCD driver level
246, 273	V_{12L}, V_{12R}	-	Power supply for LCD driver level
247, 272	V_{43L}, V_{43R}	-	Power supply for LCD driver level
248, 271	V_{5L}, V_{5R}	-	Power supply for LCD driver level
269	V_{SS}	-	Display data shift direction selection
250	V_{DD}	-	Power supply for logic circuit(+2.5 to +5.5V)
251	S/C	I	Segment mode/common mode selection
252	EIO_2	I/O	Input/output for chip select or data of shift register
253 to 259	DI_0-DI_6	I	Input display of data it for segment mode
260	DI_7	I	Input of display data in Segment mode, or Dual mode data input in common mode.
261	XCK	I	Display data shift clock input for segment mode
262	$\overline{DISPOFF}$	I	control pin input for deselect output
263	LP	I	Latch pulse input/shift clock input for shift register in segment mode
264	EIO_1	I/O	Input/output for chip select or data of shift register in segment mode
265	FR	I	AC-converting signal for LCD driver waveform
266	L/R	I	Mode selection input
267	MD	I	Test mode selection
268	$TEST_1$	I	Test mode selection
1, 242,243, 249, 270, 276	Dummy	-	Dummy PADS

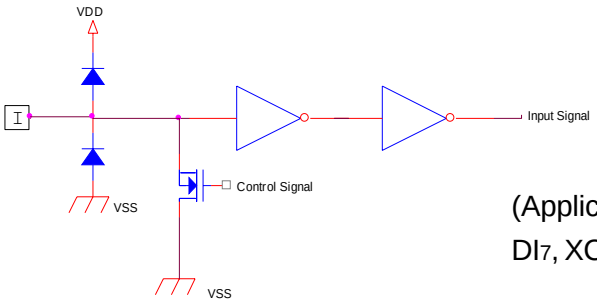
Tab.1

Input/Output Circuit



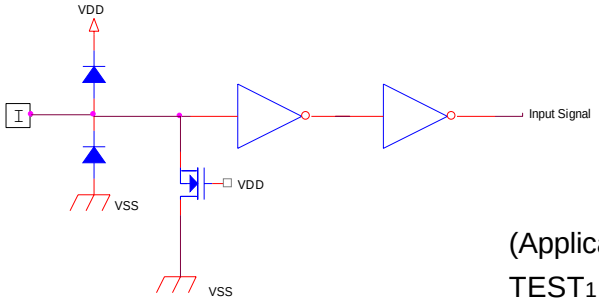
(Applicable pins)
L/R, S/C, DI_0~DI_6,
$\overline{DISPOFF}$, LP, FR, MD

Fig.3 Input Circuit(1)



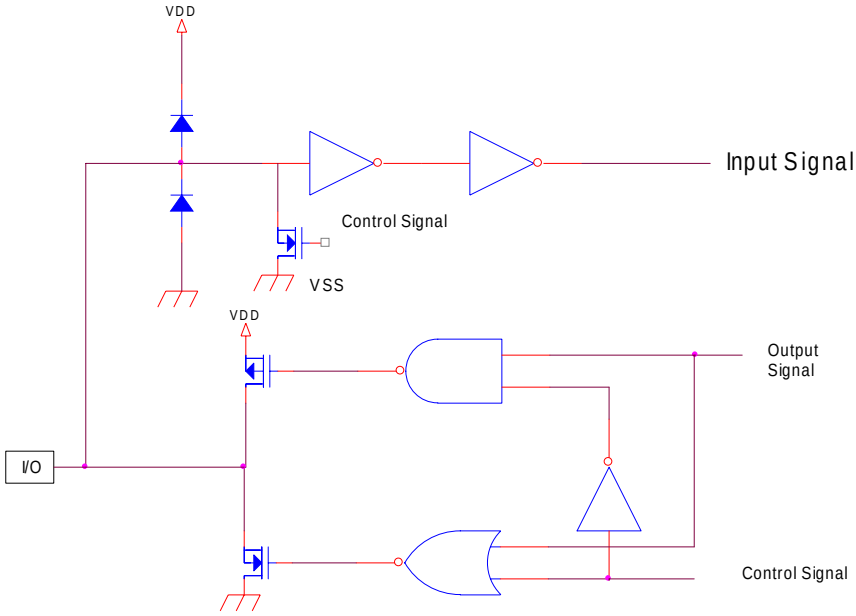
(Applicable pins)
DI_7, XCK

Fig.4 Input Circuit(2)



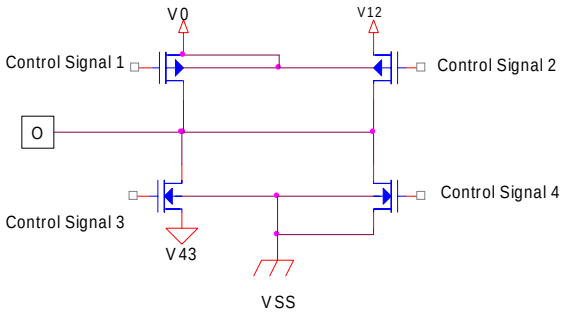
(Applicable pins)
$TEST_1$

Fig.5 Input Circuit(3)



(Applicable pins)
EIO_1, EIO_2

Fig.6 Input/Output Circuit



(Applicable pins)
Y_1 to Y_{240}

Fig.7 LCD Driver Output Circuit

Pin Functions
(Segment mode)

Symbol	Function
V_{DD}	Logic circuit power supply +2.5 to +5.5 V
V_{SS}	Ground pin
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply for LCD driver voltage level ● Normally, the bias voltage used is set by a resistor divider. ● Ensure that voltages are set such that $V_{SS}<V_5<V_{43}<V_{12}<V_0$. ● To further reduce the difference between the output waveforms of LCD. driver output pins Y_1 and Y_{240} should be externally connected to V_{iR} and V_{iL} (i=0, 12, 43, 5).
DI_0~DI_7	Input for display data ● In 4-bit parallel input mode, input data into the 4 pins DI_0~DI_3 Connect DI_4-DI_7 to V_{SS} or V_{DD}. ● In 8-bit parallel input mode, input data into the 8 pins DI_0~DI_7.
XCK	Input clock pin for displaying data ● Data is read on the falling edge of the clock pulse.
LP	Latch pulse input for displaying data ● Data is latched on the falling edge of the clock pulse.
L/R	Direction selection for reading display data ● When set to V_{SS} , data is read sequentially from Y_{240} to Y_1. ● When set to V_{DD}, data is read sequentially from Y_1 to Y_{240}.
$\overline{DISPOFF}$	Control input to deselect output level ● The input signal is level-shifted from logic voltage level to LC drive voltage level and control LC drive circuit. ● When set to Vss level "L", the LCD driver output pins (Y_1~Y_{240}) are set to level V_5. ● While set to "L", the contents of the line latch are cleared, but read the display data in the data latch regardless of condition of $\overline{DISPOFF}$. When the $\overline{DISPOFF}$ function is cancelled, the driver outputs deselect level (V_{12} or V_{43}), then outputs the contents of the data latch on the next falling edge of the LP. At that time, if $\overline{DISPOFF}$ removal time does not meet the conditions shown in conditions, it can not output the reading data correctly.
FR	AC signal for LCD driver output level ● The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. ● Normally, inputs a frame inversion signal. ● The LCD driver output pin's output voltage level can be set using the line latch output signal and the FR signal. ● Truth table is shown on page10.

Tab.2

Pin Functions

(Segment mode)

Symbol	Function
MD	Mode selection ● When set to V_{DD} level "L", 4-bit parallel input mode is selected. ● When set to V_{SS} level "H", 8-bit parallel input mode is selected. ● The relationship between the display data and driver output pins is shown on page11.12.13.
S/C	Segment mode/common mode selection pin ● When set to V_{DD}, segment input mode is set.
EIO1 EIO2	Input/Output for chip selection ● When L/R input is at V_{SS} level "L", EIO_1 is set for output, and EIO_2 is set for input. ● When L/R input is at V_{DD} level "H", EIO_1 is set for input, and EIO_2 is set for output. ● During output, set to "H" while LP*XCK is "H" After 240-bit data have been read, set to "L" for one cycle (from falling edge of XCK), after which it returns to "H". ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 240-bits of data have been read, the chip is deselected.
TEST1	Test mode selection ● During nomal operation, tie to Vss level "L".
Y_1-Y_{240}	LCD driver output ● Corresponding directly to each bit of the data latch, one level(V0, V12, V43, or V_5) is selected for output. ● Truth table values is shown on page10.

Tab.3

Pin Functions
(Common mode)

Symbol	Function
V_{DD}	Logic circuit power supply pin connects to +2.5 to +5.5 V.
V_{SS}	Ground pin.
V_{0R}, V_{0L} V_{12R}, V_{12L} V_{43R}, V_{43L} V_{5R}, V_{5L}	Power supply pin for LCD driver voltage bias ● Normally, the bias voltage used is set by a resistor divider ● Ensure that voltages are set such that ($V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$) ● To further reduce the difference between the output waveforms of LCD driver output pins Y_1 and Y_{240}, externally connect V_{iR} and V_{iL}(i=0, 12, 43, 5).
EIO_1	Bidirectional shift register input/output. ● Output when L/R is set at Vss level "L", input when L/R is at V_{DD} level "H". ● When EIO_1 is used as input pin, it will be pulled-down. ● When EIO_1 is used as output pin, it not be pulled-down.
EIO_2	Bidirectional shift register input/output. ● Input when L/R is set at V_{SS} level "L". output when L/R is at V_{DD} . ● When EIO_2 is used as input, it will be pulled-down. ● When EIO_2 is used as output, it will not be pulled-down.
LP	Bidirectional shift register clock pulse input ● Data is shifted on the falling edge of the clock pulse.
L/R	Bidirectional shift register shift direction selection ● When set to V_{SS} data is shifted from Y_{240} to Y_1. ● When set to V_{DD}, data is shifted from Y_1 to Y_{240}.
$\overline{DISPOFF}$	Control input pin to deselect output level ● The input signal is level-shifted from logic voltage level to LC drive voltage level, and controls LC drive circuit. ● When set to "L", the LCD driver output pins (Y_1-Y_{240}) are set to level V_{SS}. ● While set to "L", the contents of the shift resister are cleared. When the $\overline{DISPOFF}$ function is canceled, the driver outputs deselect level (V_{12} or V_{43}). and the shift data is read on the falling edge of the LP. At that time, if the $\overline{DISPOFF}$ removal time does not meet the conditions shown in Page 25, then the shift data is not read correctly.
FR	AC signal input for LCD driver output level ● The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LC drive circuit. ● The LCD driver output voltage level can be set by using the shift register output signal and the FR signal. ● Truth table is shown on page 10.

Tab.4

Pin Functions
(Common mode)

Symbol	Function
MD	Mode selection ● When set to Vss level "L", Single Mode operation is selected, when set to V_{DD} level "H", Dual Mode operation is selected.
DI_7	Dual Mode data input ● According to the data shift direction of the data shift register, data can be input starting from the 81st bit ● When the chip is used as Dual Mode, DI_7 will be pulled-down. ● When the chip is used as Single Mode, DI_7 will not be pulled-down.
S/C	Segment mode/common mode selection ● When set to V_{SS} level "L", Common Mode is set.
DI_0~DI_6	Not used ● Connect DI_0~DI_6 to V_{SS} or V_{DD}. Avoiding floating.
XCK	Not used ● XCK is pull-down in common mode, so connect them to Vss or open.
$TEST_1$	Test mode select ● During nomal operation, tie to V_{SS} level "L".
Y_1~Y_{240}	LC driver output ● Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_5)is selected. ● Truth table is shown on page10.

Tab.5

Functional Operations

Truth Table

(Segment Mode)

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level(Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_5
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H:$V_{DD}$ (+2.5 to +5.5V), L:V_{SS}(0 V)

X:Don't care

Tab.6

(Common Mode)

FR	Latch Data	$\overline{DISPOFF}$	Driver Output Voltage Level(Y_1-Y_{240})
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_5
X	X	L	V_5

Here, $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$, H:$V_{DD}$ (+2.5 to +5.5V), L:V_{SS}(0 V)

X:Don't care

Tab.7

Note:There are two kinds of power supply (logic level voltage, LC drive voltage) for LCD to each power pin specification.

"Don't care" should be connected to "H" or "L". Do not leave them open.

Relationship between the Display Data and Driver Output pins

(Segment Mode)

(a)8-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of Clock						
					60 clock	19 clock	18 clock	.....	3 clock	2 clock	1 clock
L	L	Output	Input	DI_0	Y_1	Y_9	Y17	.....	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	.....	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	.....	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y20	.....	Y_{220}	Y_{228}	Y_{236}
				DI4	Y_5	Y13	Y21	.....	Y_{221}	Y_{229}	Y_{237}
				DI5	Y_6	Y_{14}	Y22	.....	Y_{222}	Y_{230}	Y_{238}
				DI6	Y_7	Y_{15}	Y23	.....	Y_{223}	Y_{231}	Y_{239}
				DI7	Y_8	Y_{16}	Y24	.....	Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	.....	Y24	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	.....	Y23	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	.....	Y22	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	.....	Y21	Y_{13}	Y_5
				DI4	Y_{236}	Y_{228}	Y_{220}	.....	Y20	Y_{12}	Y_4
				DI5	Y_{235}	Y_{227}	Y_{219}	.....	Y_{19}	Y_{11}	Y_3
				DI6	Y_{234}	Y_{226}	Y_{218}	.....	Y_{18}	Y_{10}	Y_2
				DI7	Y_{233}	Y_{225}	Y_{217}	.....	Y_{17}	Y_9	Y_1

Tab.8

(b)4-bit Parallel Mode

MD	L/R	EIO_1	EIO_2	Data Input	Figure of Clock						
					60 clock	59 clock	58 clock	.....	3 clock	2 clock	1 clock
H	L	Output	Input	DI_0	Y_1	Y_5	Y_9	.....	Y_{229}	Y_{233}	Y_{237}
				DI_1	Y_2	Y_6	Y_{10}	.....	Y_{230}	Y_{234}	Y_{238}
				DI_2	Y_3	Y_7	Y_{11}	.....	Y_{231}	Y_{235}	Y_{239}
				DI_3	Y_4	Y_8	Y_{12}	.....	Y_{232}	Y_{236}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{236}	Y_{232}	.....	Y_{12}	Y_8	Y_4
				DI_1	Y_{239}	Y_{235}	Y_{231}	.....	Y_{11}	Y_7	Y_3
				DI_2	Y_{238}	Y_{234}	Y_{230}	.....	Y_{10}	Y_6	Y_2
				DI_3	Y_{237}	Y_{233}	Y_{229}	.....	Y_9	Y_5	Y_1

Tab.9

(Common Mode)

MD	L/R	Data Transfer Direction	EIO1	EIO2	DI7
L (Single)	L(shift to left)	$Y_{240} \rightarrow Y_1$	Output	Input	x
	H(shift to right)	$Y_1 \rightarrow Y_{240}$	Input	Output	x
H (Dual)	L(shift to left)	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H(shift to right)	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Input	Output	Input

Tab.10

L: V_{SS}(0 V), H: V_{DD} (+2.5V to +5.5V), x: Don't Care

Note: "Don't care" should be connected to "H" or "L". Do not leave them open.

Connection Examples of Plural Segment Drives

(a) Case of L/R="L"

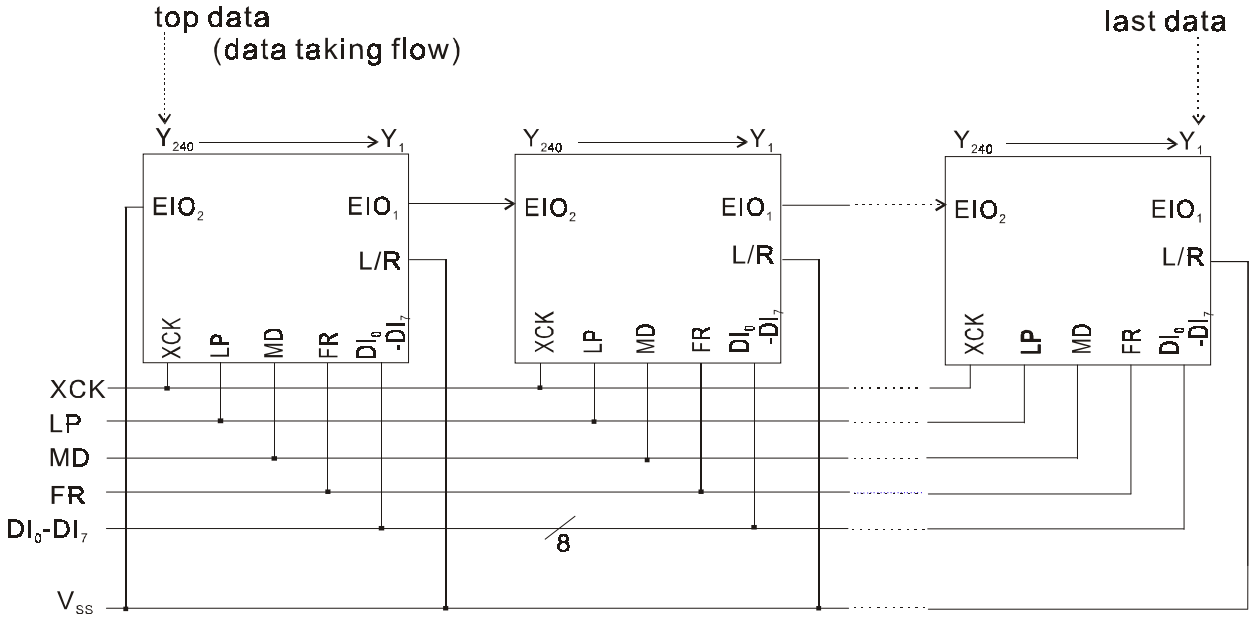


Fig.8

(b) Case of L/R="H"

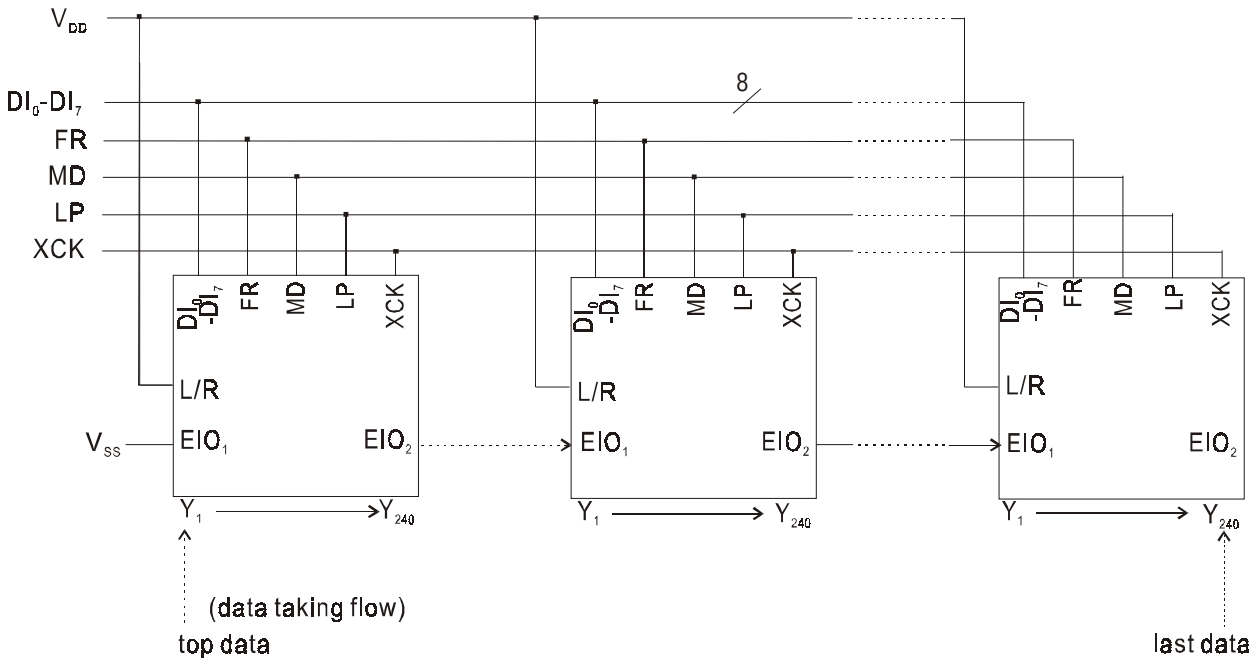


Fig.9

Timing Chart of 4-Device cascade Connection of Segment Drivers

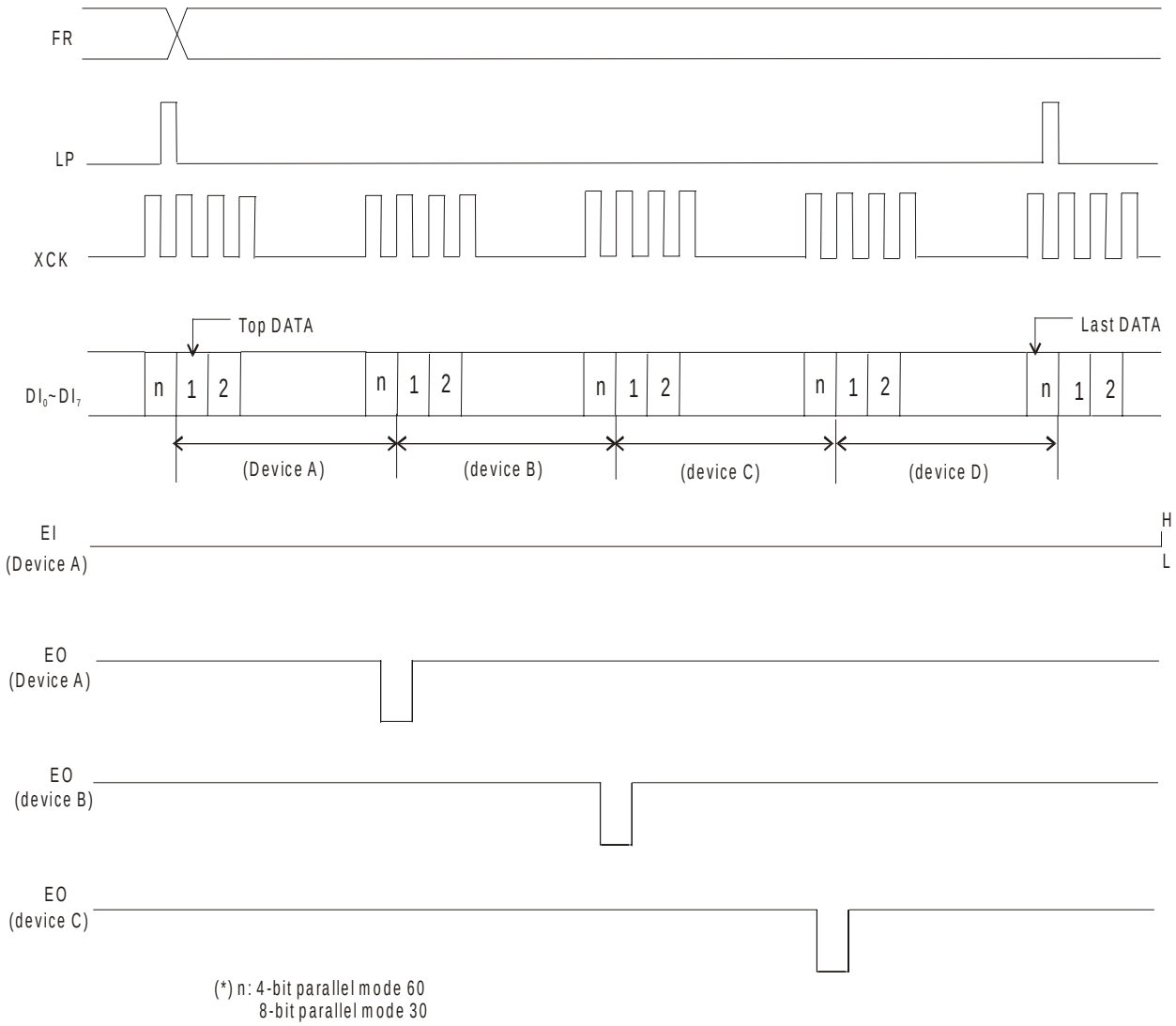


Fig.10

Connection Examples for Plural Common Drivers

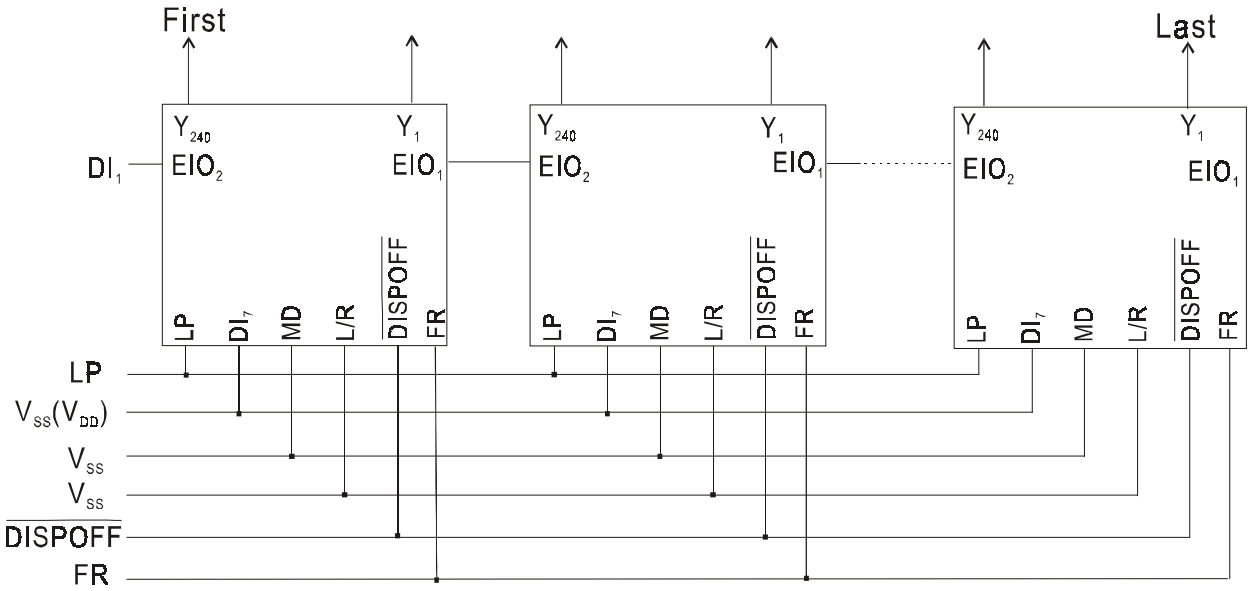


Fig.11 Single Mode (Shifting toward left)

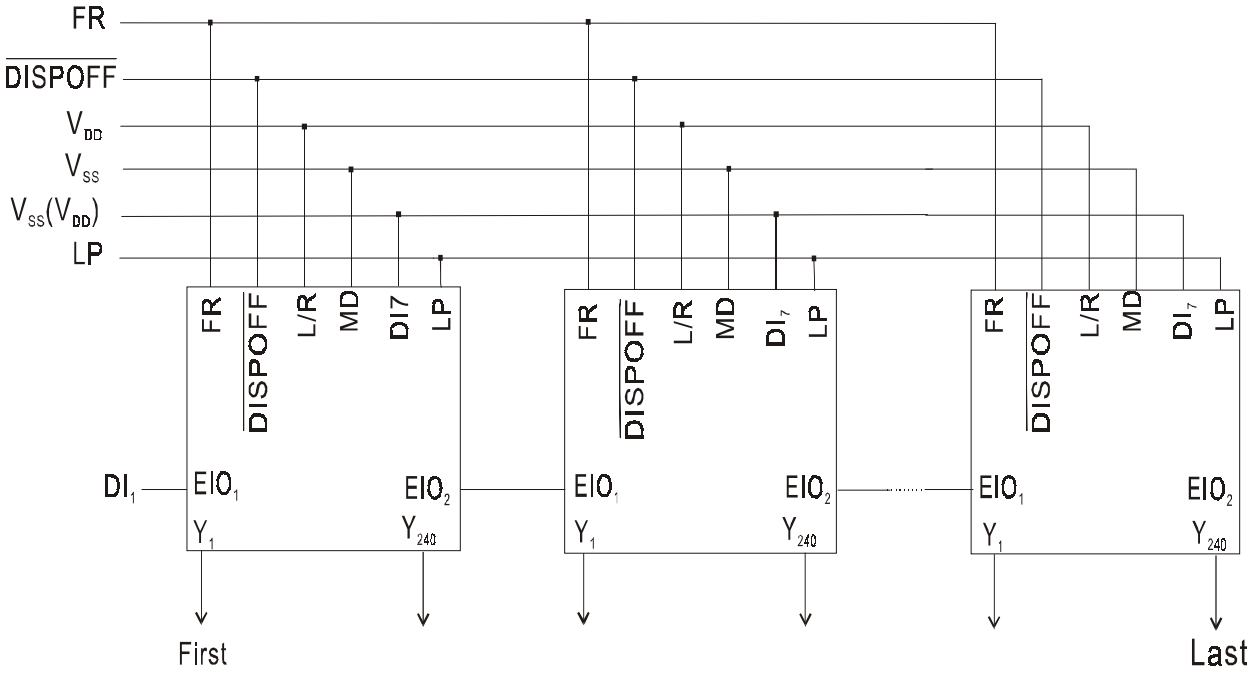


Fig.12 Single Mode (Shifting toward right)

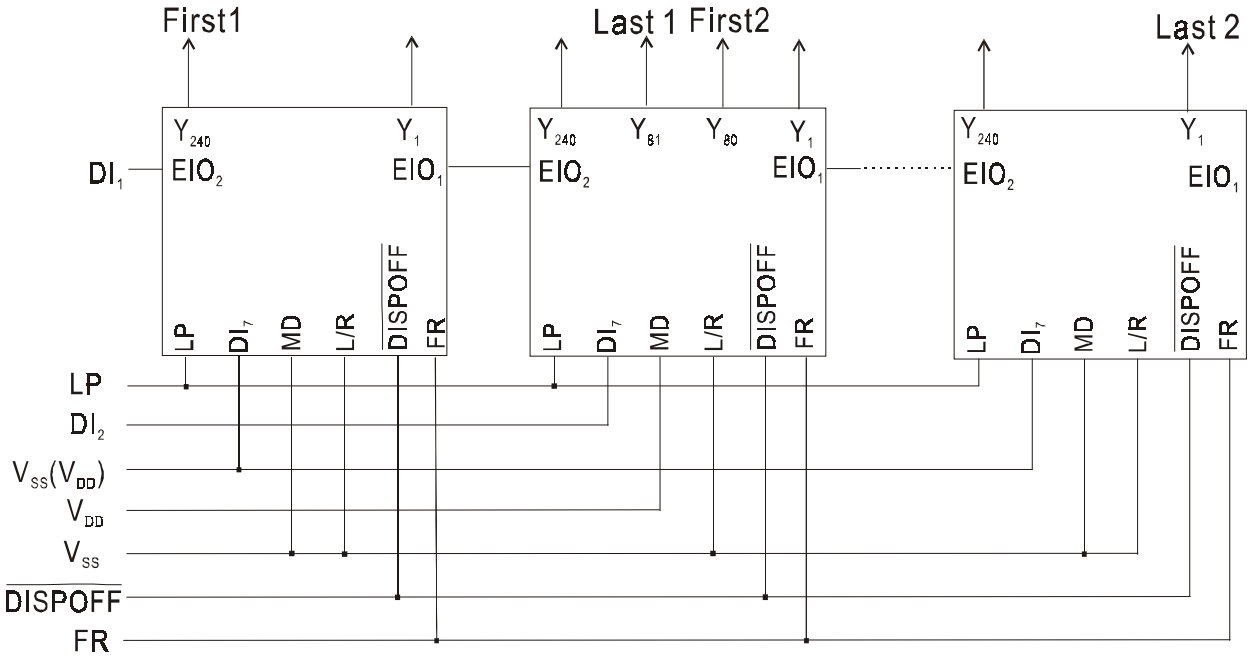


Fig.13 Dual Mode (Shifting toward left)

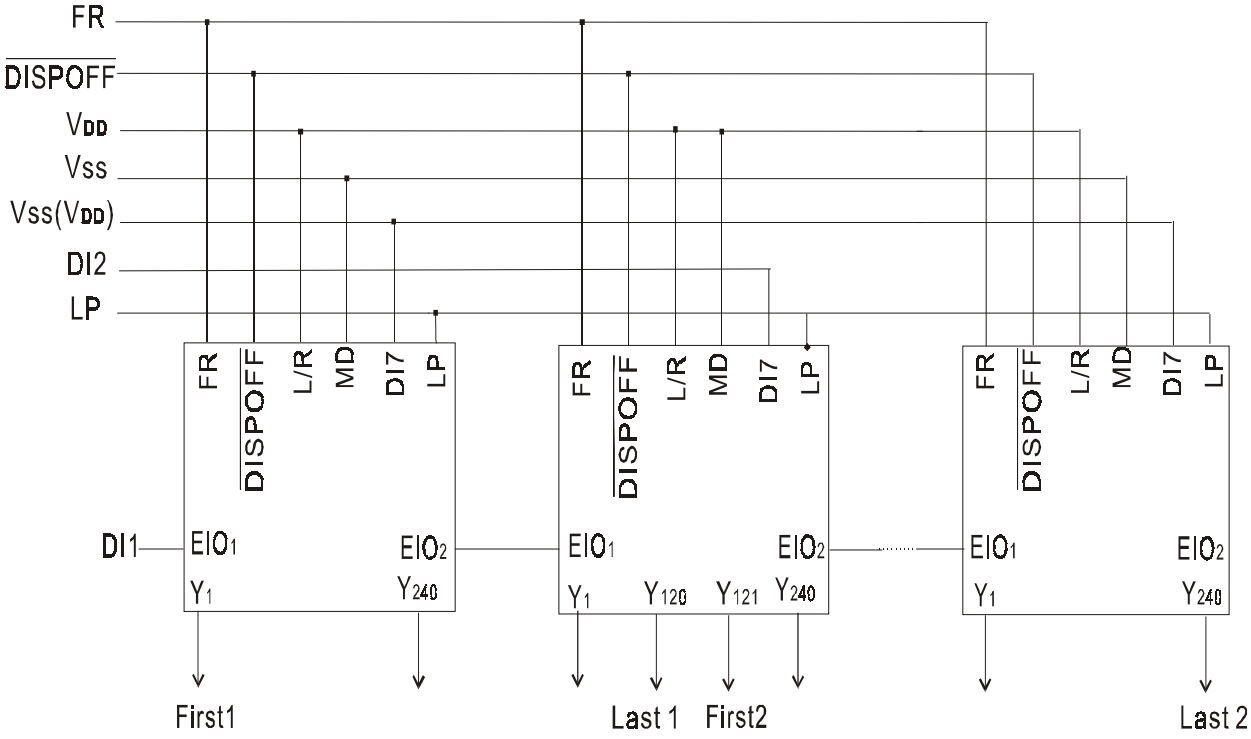


Fig.14 Dual Mode (Shifting toward right)

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Applicable Pins	Ratings	Unit
Supply voltage(1)	V_{DD}	Ta=25°C Referenced to V_{SS}(0 V)	V_{DD}	-0.3 to +7.0	V
Supply voltage(2)	V_0		V_{0L},V_{0R}	-0.3 to +45.0	V
	V_{12}		V_{12L},V_{12R}	-0.3 to V_0+0.3	V
	V_{43}		V_{43L},V_{43R}	-0.3 to V_0+0.3	V
	V_5		V_{5L},V_{5R}	-0.3 to V_0+0.3	V
Input voltage	V_1		DI_{0-7}, XCK, LP, L/P, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	-0.3 to V_{DD}+0.3	V
Storage temperature	Tstg			-45 to +125	°C

Tab.11

Recommended Operating Conditions

Parameter	Symbol	Conditions	Applicable pins	Min.	Typ.	Max.	Unit
Supply voltage(1)	V_{DD}	Referenced to V_{SS} (0 V)	V_{DD}	+2.5		+5.5	V
Supply voltage(2)	V_0		V_{0L}, V_{0R}	+15.0		+40	V
Storage temperature	T_{opr}			-20		+85	°C

Tab.12

Note:Ensure that voltages are set such that $V_{SS} \le V_5 < V_{43} < V_{12} < V_0$.

Electrical Characteristics

DC Characteristics

(Segment Mode)

(V_{SS}=V_5=0 V, V_{DD}=+2.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}			$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	0.8V_{DD}			V
	V_{IL}						0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1,EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}		$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			+10.0	μA
	I_{LIL}	V_I=V_{SS}					-10.0	μA
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V	V_0=+40.0V	$Y_1\sim Y_{240}$		1.0	1.5	KΩ
			V_0=+30.0V			1.5	2.0	
			V_0=+20.0V			2.0	2.5	
Stand-by current	I_{STB}	*1		Vss			75.0	μA
Consumed current(1) (Deselection)	I_{DD1}	*2		V_{DD}			2.0	mA
Consumed current(2) (Selection)	I_{DD2}	*3		V_{DD}			12.0	mA
Consoumed current	I_0	*4		V_0			1.5	mA

Tab.13

Note:

*1 V_{DD}=+5.0V, V_0=+40V, V_I=V_{SS}.

*2 V_{DD}=+5.0V, V_0=+40V, f_{XCK}=14MHz, No-load, EI=V_{DD}.
The input data is turned over by data taking clock (4-bit parallel input mode)

*3 V_{DD}=+5.0V, V_0=+40V, f_{XCK}=14MHz, No-load, EI=V_{SS}.
The input data is turned over by data taking clock (4-bit parallel input mode).

*4 V_{DD}=+5.0V, V_0=+40V, f_{XCK}=14MHz, f_{LP}=41.6KHz, f_{FR}=80Hz, No-load.
The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode)

(V_{SS}=V_5=0 V, V_{DD}=+2.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Conditions		Applicable pins	Min.	Typ.	Max.	Unit
Input voltage	V_{IH}			$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$	0.8V_{DD}			V
	V_{IL}						0.2V_{DD}	V
Output voltage	V_{OH}	I_{OH}=-0.4mA		EIO_1, EIO_2	V_{DD}-0.4			V
	V_{OL}	I_{OL}=+0.4mA					+0.4	V
Input leakage current	I_{LIH}	V_I=V_{DD}		$DI_{0\sim6}$, LP, L/R, FR, MD, S/C, $\overline{DISPOFF}$			+10.0	μA
	I_{LIL}	V_I=V_{SS}		$DI_{0\sim7}$, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, $\overline{DISPOFF}$			-10.0	μA
Input pull-down current	I_{PD}	V_I=V_{DD}		XCK,EIO_1EIO_2, DI_7			100.0	μA
Output resistance	R_{ON}	$\lvert\Delta V_{ON}\rvert$ =0.5V	V_0=+40.0V	$Y_1\sim Y_{240}$		1.0	1.5	KΩ
			V_0=+30.0V			1.5	2.0	
			V_0=+20.0V			2.0	2.5	
Stand-by current	I_{STB}	*1		Vss			75.0	μA
Consumed current(1)	I_{DD1}	*2		V_{DD}			120.0	μA
Consumed current(2)	I_{DD2}	*3		V_0			240.0	μA

Tab.14

*1 V_{DD}=+5.0V, V0=+40V, V_I=V_{SS}.

*2 V_{DD}=+5.0V, V0=+40V, f_{LP}=41.6KHz, f_{FR}=80Hz case of 1/480 duty operation, No-load.

AC Characteristics

(Segment Mode 1)

(V_{SS}=V_5=0 V, V_{DD}=+4.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r,t_f ≤ 10 ns	50			ns
Shift clock "H" pulse width	t_{WCKH}		15			ss
Shift clock "L" pulse width	t_{WCKL}		15			ns
Data setup time	t_{DS}		10			ns
Data Hold time	t_{DH}		12			ns
Latch pulse"H"pulse width	t_{WLPH}		15			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		30			ns
Latch pulse rise to Shift clock rise time	t_{LS}		25			ns
Latch pulse fall to Shift clock fall time	t_{LH}		25			ns
Input signal rise time*2	t_r				50	ns
Input signal fall time*2	t_f				50	ns
Enable setup time	t_s		10			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_D	C_L=15pF			30	ns
Output delay time(2)	t_{pd1},t_{pd2}	C_L=15pF			1.2	μs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	μs

Tab.15

Note:

*1 Take the cascade connection into consideration.

*2 (t_{CK}-t_{WCKL}-t_{WCLK}) /2 is maximum in the case of high speed operation.

(Segment Mode 2)

(V_{SS}=V_5=0 V, V_{DD}=+2.5V to +4.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r,t_f ≤ 11 ns	66			ns
Shift clock "H" pulse width	t_{WCKH}		23			ss
Shift clock "L" pulse width	t_{WCKL}		23			ns
Data setup time	t_{DS}		15			ns
Data Hold time	t_{DH}		23			ns
Latch pulse"H"pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		50			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Input signal rise time*2	t_r				50	ns
Input signal fall time*2	t_f				50	ns
Enable setup time	t_s		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_D	C_L=15pF			41	ns
Output delay time(2)	t_{pd1},t_{pd2}	C_L=15pF			1.2	μs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	μs

Tab.16

Note:

*1 Take the cascade connection into consideration.

*2 (t_{CK}-t_{WCKL}-t_{WCLK}) /2 is maximum in the case of high speed operation.

(Segment Mode 3)

(V_{SS}=V_5=0 V, V_{DD}=+2.5V to +4.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period *1	t_{WCK}	t_r,t_f ≤ 11 ns	82			ns
Shift clock "H" pulse width	t_{WCKH}		28			ss
Shift clock "L" pulse width	t_{WCKL}		28			ns
Data setup time	t_{DS}		20			ns
Data Hold time	t_{DH}		23			ns
Latch pulse "H" pulse width	t_{WLPH}		30			ns
Shift clock rise to Latch pulse rise time	t_{LD}		0			ns
Shift clock fall to Latch pulse fall time	t_{SL}		65			ns
Latch pulse rise to Shift clock rise time	t_{LS}		30			ns
Latch pulse fall to Shift clock fall time	t_{LH}		30			ns
Input signal rise time*2	t_r				50	ns
Input signal fall time*2	t_f				50	ns
Enable setup time	t_s		15			ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			μs
Output delay time(1)	t_D	C_L=15pF			57	ns
Output delay time(2)	t_{pd1},t_{pd2}	C_L=15pF			1.2	μs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	μs

Tab.17

Note:

*1 Take the cascade connection into consideration.

*2 (t_{CK}-t_{WCKH}-t_{WCKL}) /2 is maximum in the case of high speed operation.

(Timing Characteristics of Segment Mode)

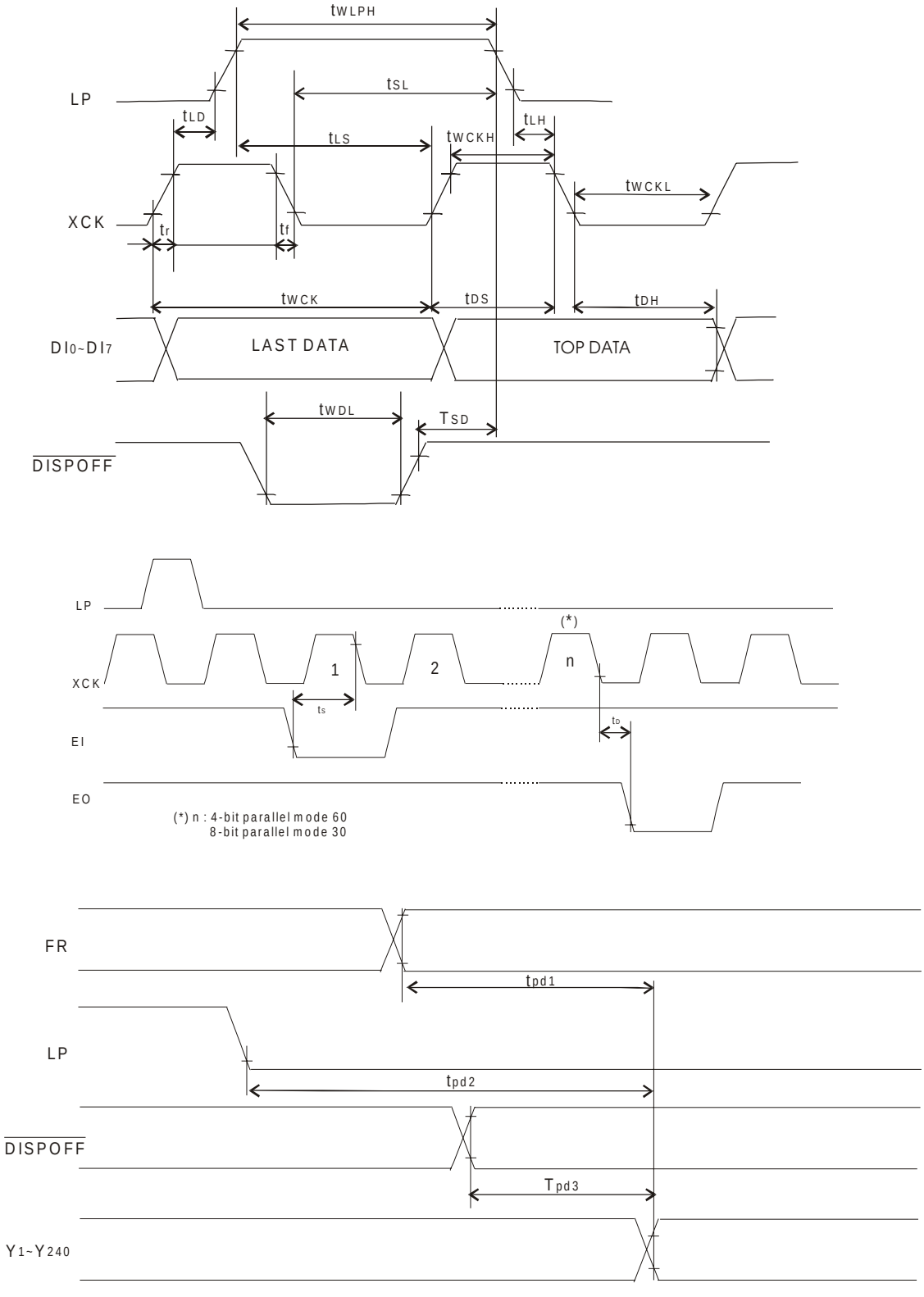


Fig.15

(Common Mode)

(V_{SS}=V_5=0 V, V_{DD}=+2.5V to +5.5V, V_0=+15.0 to +40 V, Ta=-20 to +85 ^{0}C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Shift clock period	t_{WLP}	t_r ,t_f ≤ 20 ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD}=+5.0 V±10%	15			ns
		V_{DD}=+2.5V~ +4.5V	30			
Data setup time	t_{SU}		30			ns
Data Hold time	t_H		50			ns
Input signal rise time	t_r				50	ns
Input signal fall time	t_f				50	ns
$\overline{\text{DISPOFF}}$ removal time	t_{SD}		100			ns
$\overline{\text{DISPOFF}}$ " L" pulse width	t_{WDL}		1.2			µs
Output delay time(1)	t_{DL}	C_L=15pF			200	ns
Output delay time(2)	t_{pd1}, t_{pd2}	C_L=15pF			1.2	µs
Output delay time(3)	t_{pd3}	C_L=15pF			1.2	µs

Tab.17

(Timing Characteristics of Common Mode)

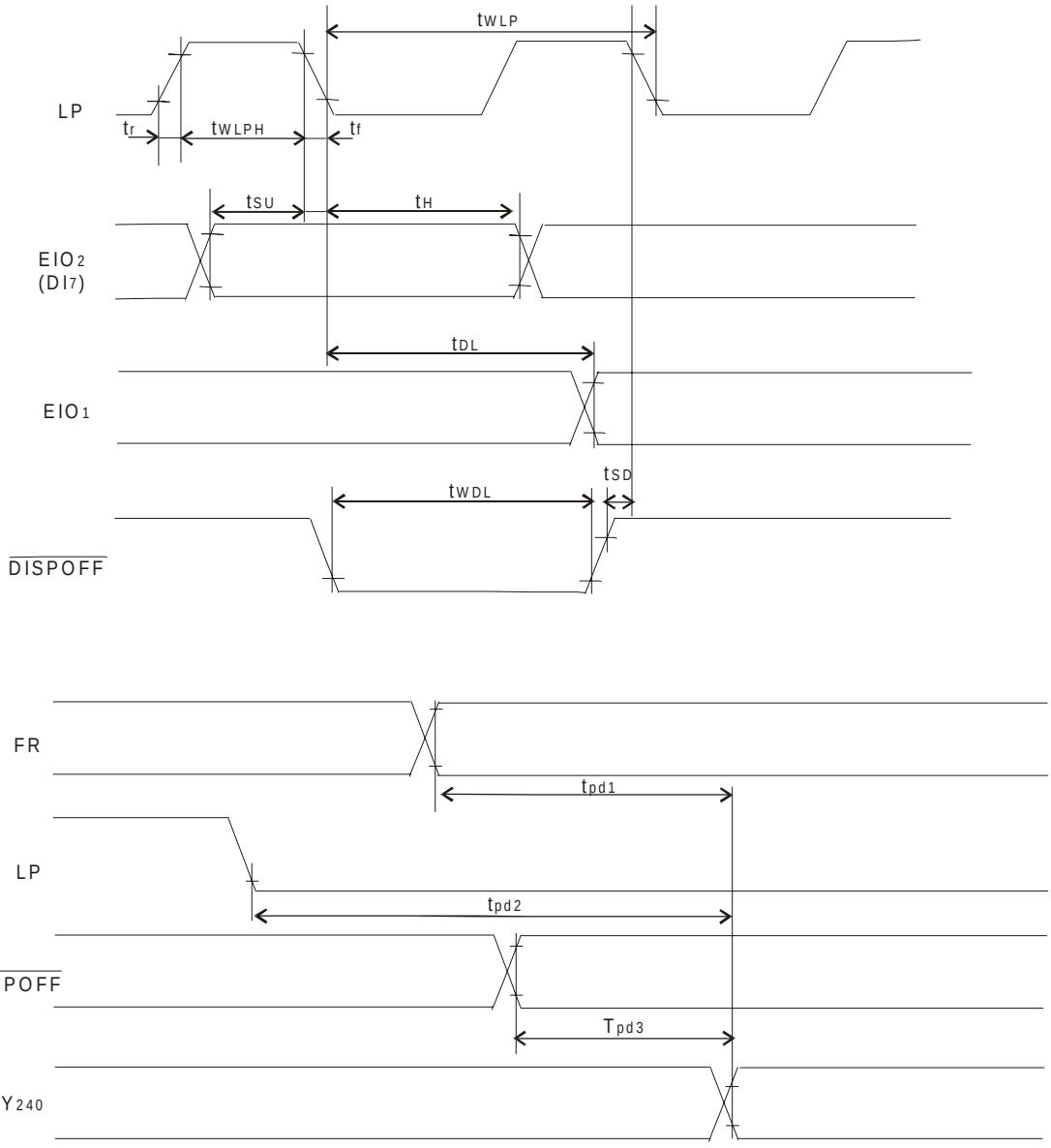


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Fig.16

Example of system Configuration

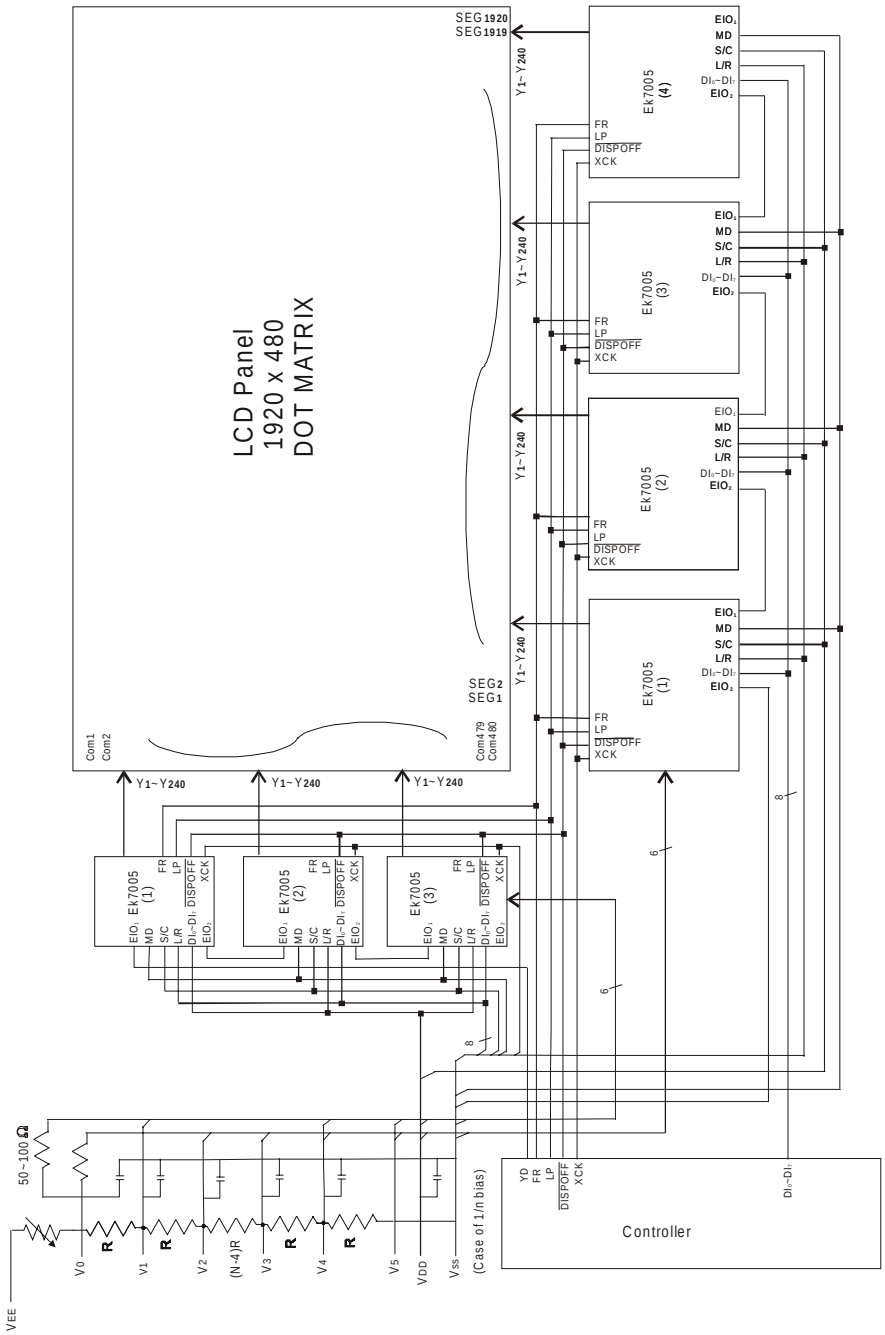

Fig.17

Example of Typical Characteristic

Parameter	Condition	Min.	Typ.	Max.	Unit
Typical Fundamental Rating Propagation Delay Time	Ta=+2.5^{0}C , Vss=0V, V_{DD}=+5.0V		10		ns

Tab.18

Precaution

- Precaution when connecting or disconnecting the power
  This LSI has a high-voltage LC driver, so it may be permanently damaged by a high current which may flow if a voltage is supplied to the LC driver power supply while the logic system power supply is floating. The detail is as follows.

- When connecting the power supply, connect the LC drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LC drive power.

- We recommend you connecting the serial resistor(50~100Ω) or fuse to the LC drive power V_0 of the system as a current limitter. And set up the suitable value of the resistor in consideration of LC display grade.

And when connecting the logic power supply, the logic condition of this LSI inside is insecurity. Therefore connect the LC drive power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that. cancel the $\overline{\text{DISPOFF}}$ function after the LC drive power supply has become stable. Furthermore, when disconnecting the power, set the LC drive output pins to level V_5 on $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LC drive power. When connecting the power supply, show the following recommend sequence.