

# HD66131ST

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Microcomputer Product Marketing Dept.,  
Microcomputer & ASIC Business Operation,  
Hitachi, Ltd.

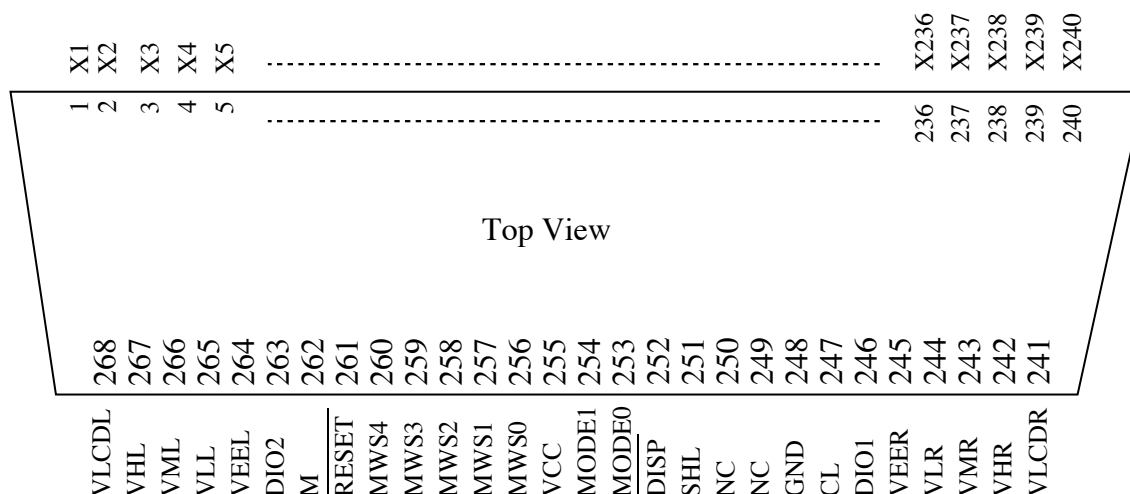
## High-Voltage Durable 240-Channel Common Driver for Dot-Matrix STN LCD

The HD 66131ST is a 240-channel common driver which drives a dot matrix STN LCD panel. By changing the mode, this can be applied to 240- and 200- and 160- channel output. Through the use of a 43-V high-voltage durable microprocessor, a high-voltage drive of +21.5 V and -21.5 V, centering on VM is possible. Low logic-drive voltage (3 V) is used. This device is used together with the segment driver HD66130T or HD66134ST.

### Features

- Display duty: Up to 1 / 240
- LCD drive voltage: 43 V max
- Number of LCD drive circuit: 240
- Operating voltage: 2.8 to 5.5 V
- Intermediate voltage I/F
- Together with the segment drivers HD66130T , HD66134ST
- Built-in alternating signal generation circuit  
Pin programmable
- Output mode change: 240-output mode  
200-output mode  
160-output mode
- Built-in display-off function
- Flex TCP

### Pin Arrangement



Note: The shape above does not indicate the actual outline.

## Internal Block Diagram

### 1. LCD drive circuit

This circuit selects and outputs the three level signals for the LCD drive. By a combination of the data in the shift register and M, either VH, VL, or VM is selected and transmitted to the output circuit.

### 2. Level shifter

This boosts a 5-V signal to a high-voltage signal for LCD drive.

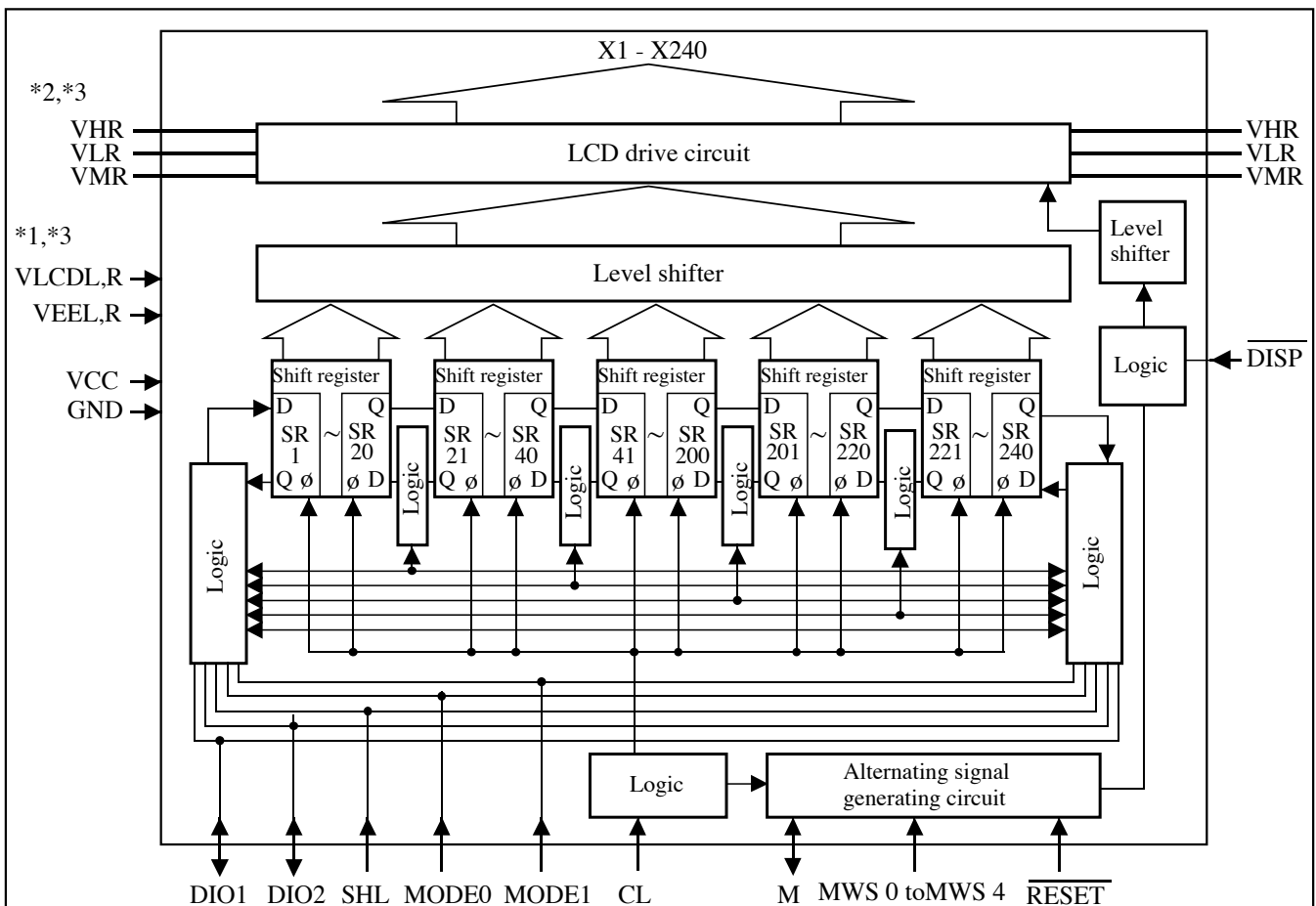
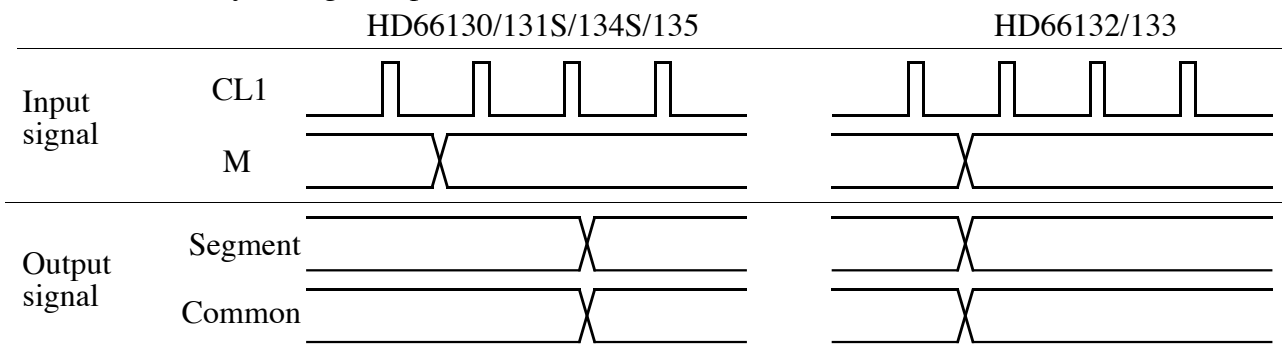
### 3. Shift register

This is a 240-bit bidirectional shift register circuit. The first line marker signal output from the DIO1 pin and DIO2 pin is sequentially shifted by shift clock CL. The shift direction is determined by the SHL pin.

### 4. Alternating signal generating circuit

This circuit generates an alternating signal (M signal) for LCD display. To suppress cross-talk, the signal is alternated in a unit from several lines to several tens of lines. By connecting MWS0 to MWS4 pins to Vcc or GND, the desired number of signals can be alternated. When alternating signals are externally input, all pins (MWS0 to MWS4) are connected to GND.

### HIFAS Family timing Comparison



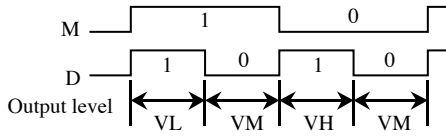
\*1 VLCDL and VLCDR, and VEEL and VEER are internally connected.

\*2 VHL and VHR, VLL and VLR, and VML and VMR are internally connected.

## Pin Functions

Classification	Symbol	Pin No.	Pin Name	I/O	Functions																																																			
Power supply	VLCDL,R VEEL,R VCC GND	268,241 264,245 255 248	VLCDL,R VEEL,R VCC GND	-	VLCDL,R - VEEL,R : Power supply for LCD drive  VCC - GND:Power supply for logic circuit																																																			
	VHL, R VLL, R VML, R	267,242 265,244 266,243	VHL, R VLL, R VML, R	Input	Power supply for LCD drive level VHL,R : Selected level (Set to the same voltage as VLCDDL, R.) VLL,R : Selected level (Set to the same voltage as VEEL, R.) VML,R : Non-selected level																																																			
	CL	247	Clock	Input	Shift clock input. Data is shifted at the falling edge of shift clock CL of the shift register.																																																			
Control signal	M	262	M	I/O	Inputs or outputs the alternating current for LCD drive output.																																																			
	MODE0 MODE1	253 254	MODE0 MODE1	Input	Switch terminals for the number of LCD drive output pins. <table border="1"> <thead> <tr> <th>MODE0</th> <th>MODE1</th> <th>Shift direction</th> </tr> </thead> <tbody> <tr> <td>" H "</td> <td>" H "</td> <td>240 - output ( X1,X2,X3.....X238,X239,X240 )</td> </tr> <tr> <td>" H "</td> <td>" L "</td> <td>200 - output ( X21,X22,X23.....X218,X219,X220 )</td> </tr> <tr> <td>" L "</td> <td>" H "</td> <td>160 - output ( X41,X42,X43.....X198,X199,X200 )</td> </tr> <tr> <td>" L "</td> <td>" L "</td> <td>Prohibited</td> </tr> </tbody> </table>	MODE0	MODE1	Shift direction	" H "	" H "	240 - output ( X1,X2,X3.....X238,X239,X240 )	" H "	" L "	200 - output ( X21,X22,X23.....X218,X219,X220 )	" L "	" H "	160 - output ( X41,X42,X43.....X198,X199,X200 )	" L "	" L "	Prohibited																																				
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	SHL	251	Shift Left	Input	This pin switches shift directions. <table border="1"> <thead> <tr> <th>SHL</th> <th>MODE0</th> <th>MODE1</th> <th>Shift direction</th> </tr> </thead> <tbody> <tr> <td colspan="4" style="text-align: center;">Right shift</td> </tr> <tr> <td rowspan="3">" H " level</td> <td>" H "</td> <td>" H "</td> <td>DIO2→SR1 →••• →SR240 →DIO1</td> </tr> <tr> <td>" H "</td> <td>" L "</td> <td>DIO2→SR21 →••• →SR220 →DIO1</td> </tr> <tr> <td>" L "</td> <td>" H "</td> <td>DIO2→SR41 →••• →SR200 →DIO1</td> </tr> <tr> <td colspan="4" style="text-align: center;">Left shift</td> </tr> <tr> <td rowspan="3">" L " level</td> <td>" H "</td> <td>" H "</td> <td>DIO1→SR240 →••• →SR1 →DIO2</td> </tr> <tr> <td>" H "</td> <td>" L "</td> <td>DIO1→SR220 →••• →SR21 →DIO2</td> </tr> <tr> <td>" L "</td> <td>" H "</td> <td>DIO1→SR200 →••• →SR41 →DIO2</td> </tr> </tbody> </table> <p>SR1, SR2•••SR240 correspond to X1, X2 •••X240. Note: The 40 or 80 pins invalidated at the 200-output or 160-output mode output the non- selected level synchronized every time; release these pins.</p>	SHL	MODE0	MODE1	Shift direction	Right shift				" H " level	" H "	" H "	DIO2→SR1 →••• →SR240 →DIO1	" H "	" L "	DIO2→SR21 →••• →SR220 →DIO1	" L "	" H "	DIO2→SR41 →••• →SR200 →DIO1	Left shift				" L " level	" H "	" H "	DIO1→SR240 →••• →SR1 →DIO2	" H "	" L "	DIO1→SR220 →••• →SR21 →DIO2	" L "	" H "	DIO1→SR200 →••• →SR41 →DIO2																			
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DIO1 DIO2	246 263	DATA	I/O	Serial data input output pin <table border="1"> <thead> <tr> <th>SHL</th> <th>DIO1</th> <th>DIO2</th> </tr> </thead> <tbody> <tr> <td>" H " level</td> <td>serial output pin</td> <td>serial input pin</td> </tr> <tr> <td>" L " level</td> <td>serial input pin</td> <td>serial output pin</td> </tr> </tbody> </table>	SHL	DIO1	DIO2	" H " level	serial output pin	serial input pin	" L " level	serial input pin	serial output pin																																											
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MWS0 MWS1 MWS2 MWS3 MWS4	256 257 258 259 260	MWS0 MWS1 MWS2 MWS3 MWS4	Input	This pin specifies the cycle of the alternating signal (M signal) in the unit of the number of lines. The number of lines, which is an integer from 2 to 31, is specified as follows. Usually, specify the number of lines within a range from 10 to 31. When the HD66131T is driven by an external alternating signal, specify the number of lines as zero. <table border="1"> <thead> <tr> <th>Number of lines</th> <th>MWS4</th> <th>MWS3</th> <th>MWS2</th> <th>MWS1</th> <th>MWS0</th> <th>Line alternating waveform</th> <th>M-pin status</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>-</td> <td>Input</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>Prohibited</td> <td rowspan="5">Output</td> </tr> <tr> <td>2</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>0</td> <td>2 lines alternated</td> </tr> <tr> <td>3</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>3 lines alternated</td> </tr> <tr> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> <td>•</td> </tr> <tr> <td>31</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>1</td> <td>31 lines alternated</td> </tr> </tbody> </table> <p>1 ="Vcc", 0 ="GND"</p>	Number of lines	MWS4	MWS3	MWS2	MWS1	MWS0	Line alternating waveform	M-pin status	0	0	0	0	0	0	-	Input	1	0	0	0	0	1	Prohibited	Output	2	0	0	0	1	0	2 lines alternated	3	0	0	0	1	1	3 lines alternated	•	•	•	•	•	•	•	31	1	1	1	1	1	31 lines alternated
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3	0	0	0	1	1	3 lines alternated																																																		
•	•	•	•	•	•	•																																																		
31	1	1	1	1	1	31 lines alternated																																																		
$\overline{\text{DISP}}$	252	Disp off	Input	Setting this pin to GND sets LCD drive output X1 to X240 to the VM level.																																																				

## Pin Functions

Classification	Symbol	Pin No.	Pin Name	I/O	Functions
Control signal	$\overline{\text{RESET}}$	261	RESET	Input	Setting this pin to GND sets initializes the alternating signal (M signal) circuit. A VCC level $\overline{\text{RESET}}$ is normally used.
	NC	249 250	No Connect	Input	These are NC pins. These pins level of VCC, GND and OPEN is available.
LCD drive output	X1 to X240	1 to 240	X1 to X240	Output	<p>LCD drive output By a combination of the display data and the M signal, when <math>\overline{\text{DISP}}</math> is set to Vcc, either VH, VL, or VM is selected and transmitted to the output circuit.</p> 

Note. ) Configuring the LCD panel using the HD66131S when using the select SEGMENT driver.

The select SEGMENT driver

SEGMENT driver	Select
HD66130(320OUT)	○
HD66132(240OUT)	X
HD66134S(240OUT)	○

## Absolute Maximum Rating

Items		Symbol	Rating	Dimension	Notes
Power supply voltage	Logic circuit	VCC	- 0.3 to +7.0	V	*1 , *6
	LCD drive circuit	VLCD	- 0.3 to +25.0	V	*1 , *6
		VEE	- 20.0 to +0.3	V	*1 , *6
Input voltage (1)		VT1	- 0.3 to VCC + 0.3	V	*1 , *2
Input voltage (2)		VH	= VLCD	V	*3
Input voltage (3)		VL	=VEE	V	*4
Input voltage (4)		VM	VEE - 0.3 to VLCD + 0.3	V	*5 , *6
Operating temperature		Topr	- 30 to + 75	°C	
Storage temperature		Tstg	- 55 to + 110	°C	

\*1 Voltage from GND.

\*2 Applicable to DIO1 , DIO2 , CL , SHL , DISP , MODE0 , MODE1 , MWS0, MWS1, MWS2, MWS3, MWS4, RESET , and M pins.

\*3 Applicable to VHL, R pins.

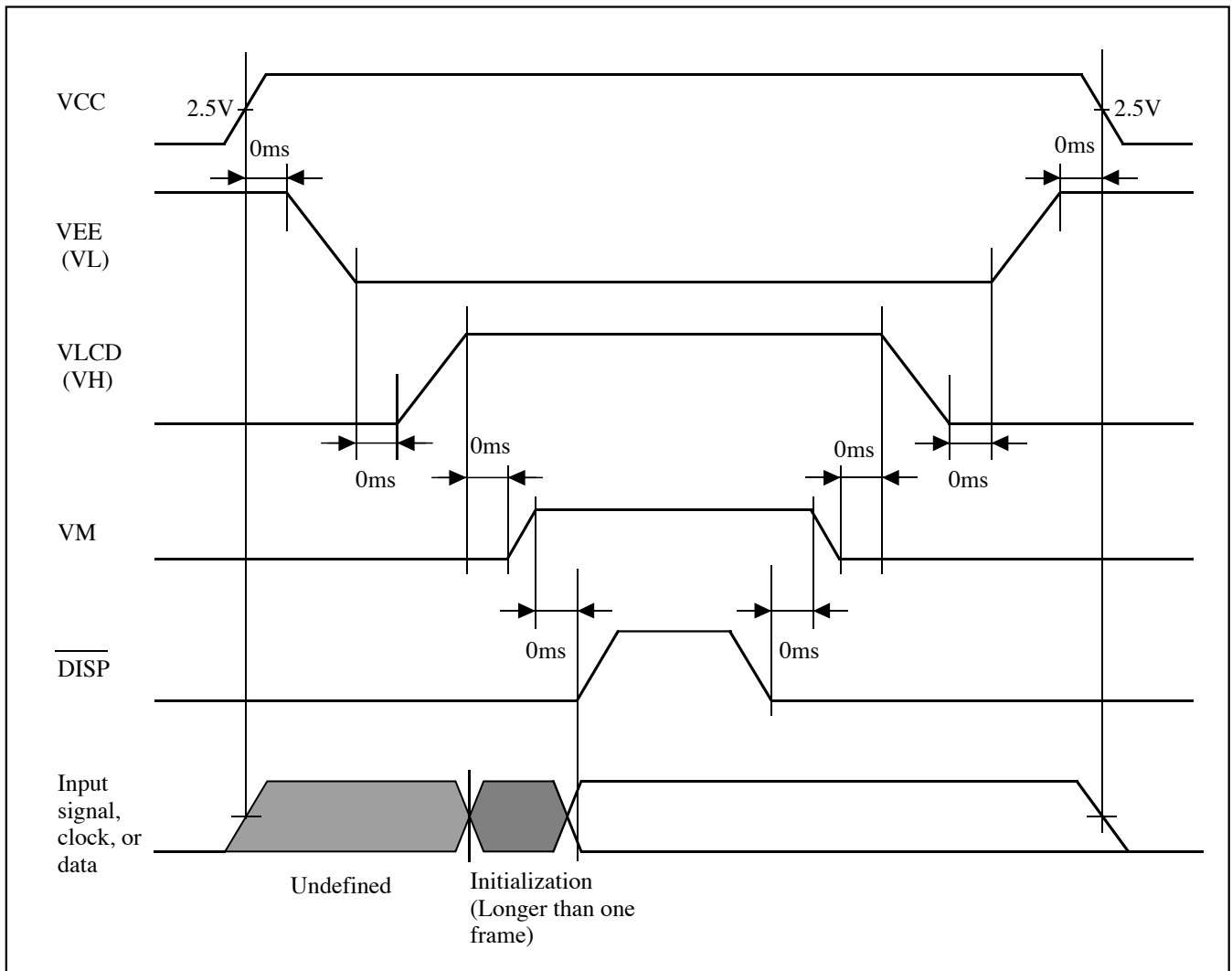
\*4 Applicable to VLL, R pins.

\*5 Applicable to VML, R pins.

(Caution)

Operating the LSI in excess of the absolute maximum rating will result in permanent damage. Use the LSI observing electrical characteristic conditions in normal operation. Exceeding the conditions will cause malfunctions or will affect LSI reliability.

- \*6 Observe the sequence of activation and inactivation for the following power supplies and signals.  
If the sequence is not observed, it may cause LSI malfunction, permanent damage, or adverse effects.



(0 ms: Minimum specification)

### 6.1 Power on

- (1) Turn on the power supply in the order of GND-VCC, GND-VEE (VL), GND-VLCD(VH), and VM. In this case, input GND to the DISP pin.
- (2) The LCD level forcibly outputs the VM level by the DISPOFF function.
- (3) The DISPOFF function has a priority even if input signal distortion occurs immediately after VCC input.
- (4) Then input the predetermined signals to initialize the driver registers. In this case, assure a period for more than one frame.
- (5) Preparation for normal display is thus completed. Cancel the DISPOFF function by setting the  $\overline{\text{DISP}}$  pin to VCC. At this point, the levels of VEE (VL), VLCD (VH) and VM must have reached the predetermined respective voltage.

### 6.2 Shut down

As a rule, shut down in order opposite to that used for power on.

- (1) Set the  $\overline{\text{DISP}}$  pin to GND.
- (2) Shut off the LCD power supply in the order of VM, GND-VLCD (VH), GND-VEE (VL).
- (3) Set VCC and the input signal to GND.

At this point, VEE (VL), VLCD (VH) and VM pin input must completely drop to 0 V.

Since the DISPOFF function is inactivated when the VCC level drops to GND, the LCD output may output a level other than VM. Therefore, an incorrect display may appear at shut down or power on.

## Electric Characteristics

DC characteristics ( $V_{CC} = 2.8$  to  $5.5$  V,  $GND = 0$  V,  $V_{LCD} - V_{EE} = 15$  to  $43$  V,  $T_a = -30$  to  $+75$  °C)

Items	Symbol	Applicable Pins	min.	typ.	max.	Dimension	Measurement Conditions	Note
Input high level voltage	$V_{iH}$	DIO1, CL, SHL, DISP, MODE0, MODE1, MWS0, MWS1	$0.8 \times V_{CC}$	-	$V_{CC}$	V		
Input low level voltage	$V_{iL}$	MWS2, MWS3, MWS4, RESET, M, DIO2	0	-	$0.2 \times V_{CC}$	V		
Output high level voltage	$V_{OH}$	DIO1, DIO2	$V_{CC} - 0.4$	-	-	V	$I_{OH} = -0.4$ mA	
Output low level voltage	$V_{OL}$	DIO1, DIO2	-	-	0.4	V	$I_{OL} = 0.4$ mA	
ON resistance between $V_i - X_j$	$R_{ON}$	X1 to X240, V pin	-	0.7	2.0	$k\Omega$	$I_{ON} = 150\mu A$	*1
Input leak current (1)	$I_{iL1}$	DIO1, CL, SHL, DISP, MODE0, MODE1, MWS0, MWS1, MWS2, MWS3, MWS4, RESET, M, DIO2	-5	-	5	$\mu A$	$V_{IN} = V_{CC}$ to GND	
Input leak current (2)	$I_{iL2}$	VH, VL, VM	-25	-	25	$\mu A$		
Current consumption (1)	ICC1	VCC	-	10	40	$\mu A$	$V_{cc}=3.3V, V_{LCD}-V_{EE}=40V$ $f_{CL}=19.2kHz, f_M=1.5kHz$	*2
Current consumption (2)	ICC2	VCC	-	20	50	$\mu A$	$V_{cc}=5.0V, V_{LCD}-V_{EE}=40V$ $f_{CL}=19.2kHz, f_M=1.5kHz$	
Current consumption (2)	ILCD	VLCD	-	20	35	$\mu A$	$V_{cc}=3.3V, V_{LCD}-V_{EE}=40V$ $f_{CL}=19.2kHz, f_M=1.5kHz$	

- \*1 This is a resistance value between the X and V pins (either of VH, VL, or VM) when a load current is applied to one of x 1 to x 240 pins. These values are regulated under the conditions of  $V_{LCD} = V_H = 23V$ ,  $V_{EE} = V_L = -17V$ ,  $V_M = 3V$ ,  $GND = 0V$ . Use VH, VL, and VM in the range of  $V_{LCD} - V_M \geq V_H - V_M = 21.5$  to  $7.5V$ ,  $V_{EE} - V_M \leq V_L - V_M = -21.5$  to  $-7.5V$ , with the relation of  $V_H > V_M > V_L$ .
- \*2 The current applied between the input and output is excluded. When an input to a CMOS gate is at an intermediate level, through current flows between the power supplies, and the power supply current increases. Therefore, use  $V_{iH} = V_{CC}$  and  $V_{iL} = GND$ .
- \*3 The voltage relationship of each signal is as follows:

Segment voltage	Segment waveform		Common waveform		Common voltage
$V_0$ (5.0 V)			VH (23.0 V)		
$V_{CC}$ (3.3 V)			VCC (3.3 V)		
$V_M$ (3.0 V)			VM (3.0 V)		
$V_1$ (1.0 V)			GND (0.0 V)		
GND (0.0 V)			VL (-17.0 V)		
	Normal display period	Off-display period	Normal display period	Off-display period	

AC characteristics (1) (VCC =2.8 to 4.5 V, GND = 0 V, VLCD - VEE = 15 to 43 V, Ta = -30 to + 75 °C)

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Clock cycle time	tCYC	CL	10	-	μs	
CL high-level width	tCWH	CL	65	-	ns	
CL low-level width	tCWL	CL	1	-	μs	
CL rising time	tr	CL	-	30	ns	
CL falling time	tf	CL	-	30	ns	
Data set-up time	tDS	DIO1,DIO2, CL	100	-	ns	
Data hold time	tDH	DIO1,DIO2, CL	50	-	ns	
Data output delay time	tDD	DIO1,DIO2, CL	-	500	ns	*1
M output delay time	tMD	M, CL	-	500	ns	*1
M set uop time	tMS	M, CL	50	-	ns	
M Hold time	tMH	M,CL	50	-	ns	
Output delay time 1	tpd1	X(n), M	-	1.2	μs	*2

AC characteristics (2) (VCC = 4.5 to 5.5 V, GND = 0 V, VLCD - VEE =15 to 43 V, Ta = - 30 to + 75 °C)

Item	Symbol	Pin Name	min.	max.	Dimensions	Note
Clock cycle time	tCYC	CL	10	-	μs	
CL high-level width	tCWH	CL	45	-	ns	
CL low-level width	tCWL	CL	1	-	μs	
CL rising time	tr	CL	-	30	ns	
CL falling time	tf	CL	-	30	ns	
Data set-up time	tDS	DIO1,DIO2, CL	100	-	ns	
Data hold time	tDH	DIO1,DIO2, CL	50	-	ns	
Data output delay time	tDD	DIO1,DIO2, CL	-	350	ns	*1
M output delay time	tMD	M, CL	-	350	ns	*1
M set uop time	tMS	M, CL	50	-	ns	
M Hold time	tMH	M,CL	50	-	ns	
Output delay time 1	tpd1	X(n), M	-	0.7	μs	*2

\*1 , \*2 The following timing is regulated with the circuit at the right connected.

