
HD66134ST

240-Channel Segment Driver for a Dot-Matrix STN Liquid Crystal Display with Low-Voltage Drive

HITACHI

Rev 1
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Description

The HD66134ST is a 240-channel segment driver that drives a dot-matrix STN liquid crystal display (LCD) panel at low voltage. The HD66134ST operates with a low 5-V LCD drive voltage and a low 3-V logic drive voltage, and it can be used together with the common driver HD66135T. The HD66134ST also incorporates a shadowing correction circuit and is suitable for high-quality image processing. The HD66134ST, packaged in a fine-pitch slim tape-carrier package (slim-TCP), makes it possible to reduce the space around the LCD panel.

Features

- Duty cycle: Up to 1/300
- LCD drive voltage: 3.5 to 5.5 V
- 240 LCD drive circuits
- Operating voltage: 2.7 to 5.5 V
- Eight data bits
- Shift clock speed
 - 25 MHz max/3 V
 - 40 MHz max/5 V
- Shadowing correction circuit
- Display-off function
- Slim-TCP
 - Output lead pitch: 70 μ m
 - User area: 5.5 mm
- Automatic generation of the chip enable signal
- Standby function

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Pin Arrangement

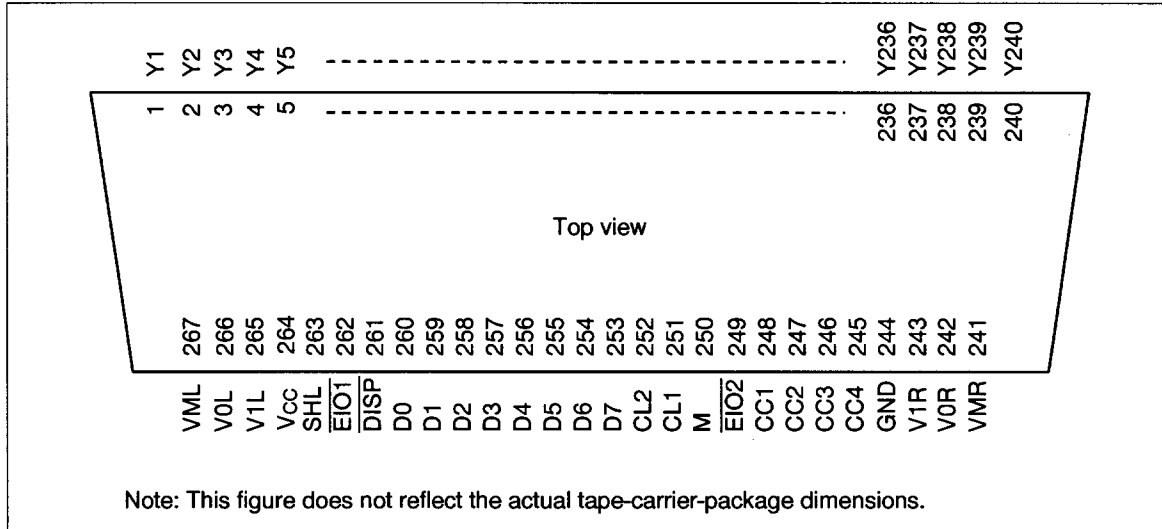


Figure 1 Pin Arrangement

Block Diagram

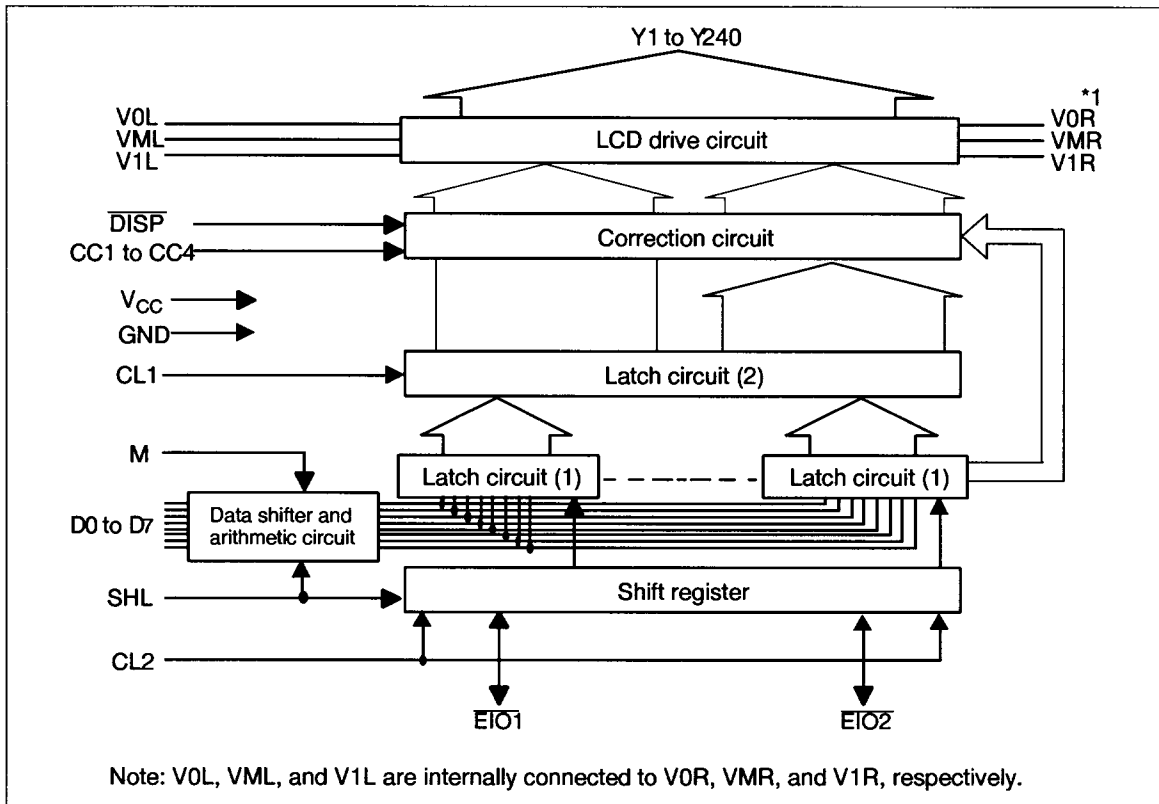


Figure 2 Block Diagram

Block Functions

LCD Drive Circuit

The 240-bit LCD drive circuit generates three voltage levels V_H, V_L, and V_M, which drive the LCD panel. One of these three levels is output to the corresponding Y pin, depending on the data in latch circuit (2), the correction signals (CC1 to CC4), and the $\overline{\text{DISP}}$ signal.

Correction Circuit

This circuit corrects the shadowing volume.

(2.1) The circuit compares the crosstalk correction signals (CC1 and CC2) from the external circuits and present output, and determines whether the effective value is increased due to crosstalk. If the effective value is increased, the output level is reset to the V_M level.

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(2.2) The circuit compares the present output data to the next output data. If there are no data changes due to the waveform distortion correction signals (CC3 and CC4), the output level is reset to the VM level.

The reset period can be adjusted by using CC1 to CC4. The correction needed depends on each output pin.

Latch Circuit (2)

A 240-bit latch circuit (2) latches data input from latch circuit (1), and outputs the latched data to the correction circuit and the LCD drive circuit, at the falling edge of each clock 1 (CL1) pulse.

Latch Circuit (1)

The 240-bit latch circuit (1) latches 8-bit parallel data input via the D0 to D7 pins, and outputs the latched data to latch circuit 2, both according to the timing generated by the shift register.

Shift Register

The 30-bit shift register generates and outputs data latch signals for latch circuit (1) at the falling edge of each clock 2 (CL2) pulse.

Data Shifter and Arithmetic Circuit

The data shifter shifts the destinations of data output when necessary. The arithmetic circuit performs operations for the data and AC signal M.

Pin Function
Table 1 Pin Functions

Classification	Symbol	Pin No.	Pin Name	Input/		Function
				Output		
Power supply	V _{CC}	264	V _{CC}	—		VCC–GND: Logic power supply
	GND	244	GND			
	V0L, V0R	266, 242	V0L, V0R	Input		LCD drive-level voltage.
	VML, VMR	267, 241	VML, VMR			See figure 3.
	V1L, V1R	265, 243	V1L, V1R			
Control signal	CL1	251	Clock 1	Input		Display data latch signal. The LCD drive signal corresponding to the display data is output at the falling edge of this signal.
	CL2	252	Clock 2	Input		Display data latch signal. Display data is latched at the falling edge of this signal.
	M	250	M	Input		Changes the LCD drive outputs to AC.
	D0 to D7	260 to 253	Data0 to Data7	Input		When the display data is 1 (V _{CC} level), the LCD drive output level is the selection level and the liquid-crystal display is on, and when it is 0 (GND level), they are non-selection level and off, respectively.
	SHL	263	Shift left	Input		A control signal to switch the data output destination. See the section on Switching the Data Output Destination.
	EIO1	262	Enable I/O 1	Input/ output		If SHL is at the GND level, $\overline{\text{EIO1}}$ inputs the chip enable signal and $\overline{\text{EIO2}}$ outputs the chip enable signal; and if it is at the V _{CC} level, the opposite occurs. Enable input: The chip enable-input pin of the first HD66134ST must be fixed to the GND level, and the other chip-enable input pins
	EIO2	249	Enable I/O 2	Input/ output		must be connected to the chip enable-output pins of the previous HD66134ST. Enable output: The chip enable-output pin must be connected to the chip enable-input pin of the next HD66134ST.
	DISP	261	Disp off	Input		A low $\overline{\text{DISP}}$ level sets LCD drive outputs Y1 to Y240 to the VM level.
	CC1	248	CoreCt 1	Input		Rising crosstalk correction signal. The V1 output pin is reset to the VM level when CC1 is high.
	CC2	247	CoreCt 2	Input		Falling crosstalk correction signal. The V0 output pin is reset to the VM level when CC2 is high.

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Table 1 Pin Functions (cont)

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function
Control signal (cont)	CC3	246	CoreCt 3	Input	Waveform distortion non-selected (black) data correction signal. The present output pin (non-selected) and the next output pin (non-selected) are reset to the VM level when CC3 is high.
	CC4	245	CoreCt 4	Input	Waveform distortion selected (white) data correction signal. The present output pin (selected) and the next output pin (selected) are reset to the VM level when CC4 is high.
LCD drive output	Y1 to Y240	1 to 240	Y1 to Y240	Output	Either level V0 or V1 is output according to the combination of the M signal and display data when the $\overline{\text{DISP}}$ pin is set at V_{CC} . See figure 4.

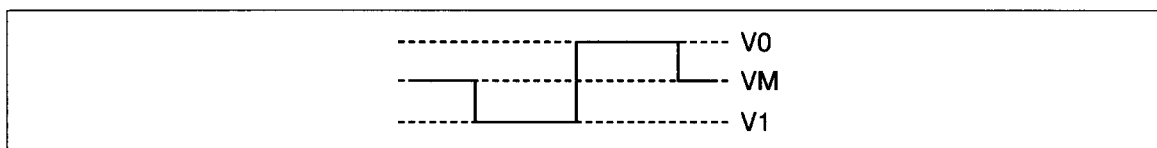


Figure 3 LCD Drive Level Voltage

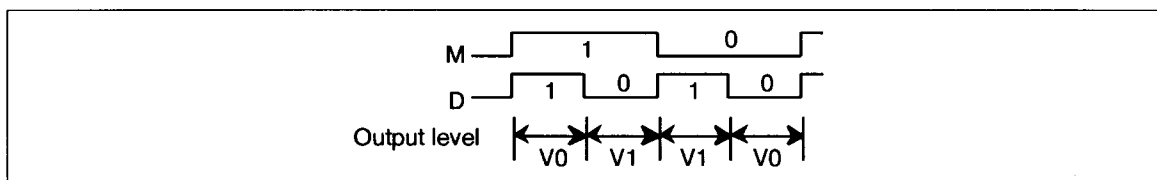


Figure 4 Selection of LCD Drive Output Level

Switching the Data Output Destination

The output destination of data latched by the SHL signal is switched left or right. At this time, the input and output of the enable signal pins can also be switched. See figure 5.

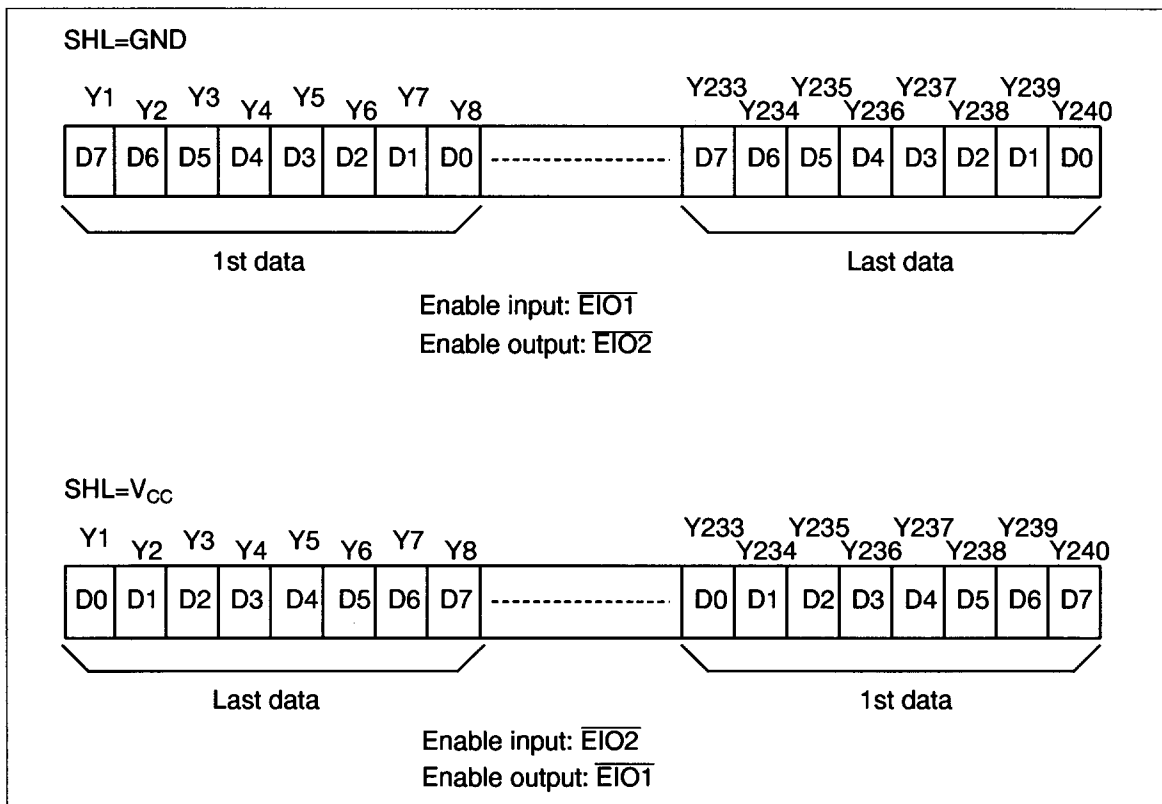


Figure 5 Data Output Destination

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Operation Timing

Figure 6 shows the 8-bit data-latch timing when $SHL = GND$; that is, when the $\overline{EIO1}$ pin is a chip-enable input and the $\overline{EIO2}$ pin is a chip-enable output. When $SHL = V_{CC}$, the $\overline{EIO1}$ pin is a chip-enable output and the $\overline{EIO2}$ pin is a chip-enable input.

When a low chip-enable signal is input via the $\overline{EIO1}$ pin, the HD66134ST is first released from the data-standby state, then, at the falling edge of the following CL2 pulse, it is released entirely from the standby state and starts latching data.

It simultaneously latches eight bits of data at the falling edge of each CL2 pulse. When it has latched 232 bits of data, it sets the $\overline{EIO2}$ signal to low. When it has latched 240 bits of data, it automatically stops and enters the standby state, initiating the next HD66134ST, provided its $\overline{EIO2}$ pin is connected to the $\overline{EIO1}$ pin of the next HD66134ST.

The HD66134STs output one line of data from the Y1 to Y240 pins at the falling edge of each CL1 pulse. Data d1 is output from Y1, and d240 from Y240 when $SHL = GND$, and d1 is output from Y240, and d240 from Y1 when $SHL = V_{CC}$.

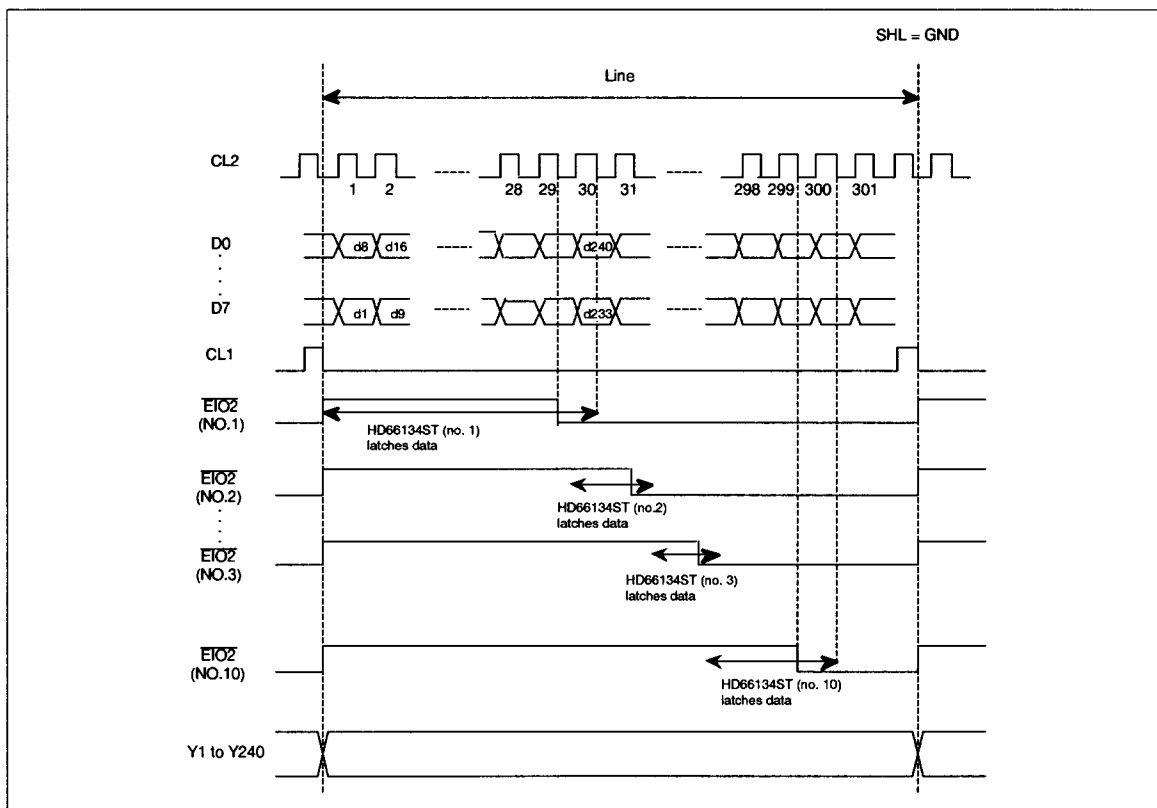


Figure 6 Data Latch Timing

Correction Circuit

The HD66134STs include shadowing correction circuits. There are two types of shadowing: one caused by crosstalk, and the other by waveform distortion. In both types, image quality can be improved by correction circuits CC1, CC2, CC3, and CC4.

(1) CC1 and CC2 (shadowing caused by crosstalk)

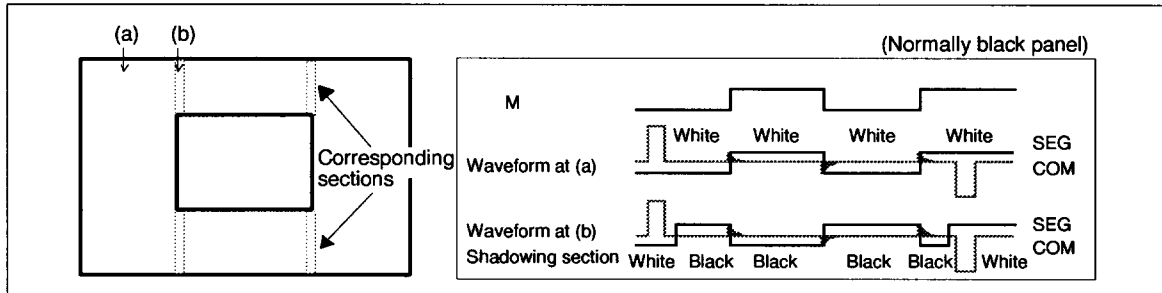


Figure 7 CC1 and CC2

When a ruled line is displayed, noise occurs in the common VM level in the LCD panel due to the segment change of a solid background in M reverse. This is because many segments display the solid background and are simultaneously changed, affecting the common VM level (creating crosstalk). The effective voltage for section (a) in the solid background becomes low. On the other hand, the effective voltage for section (b) becomes high. Shadowing occurs in the corresponding sections due to the different voltages.

The HD66134STs compare the crosstalk correction signals CC1 and CC2 and the present output, and determine whether the effective value is increased by the crosstalk. If increased, the output level is reset to the VM, which corrects the effective voltages in (a) and (b) and suppresses the shadowing. Figure 8 shows an example of the crosstalk-correction-signal external circuit. The basic potentials of a comparator ($VM + \Delta V$ and $VM - \Delta V'$) are corrected according to the shadowing level for output correction while CC1 and CC2 are high. CC1 corrects the rising crosstalk, and CC2 corrects the falling crosstalk.

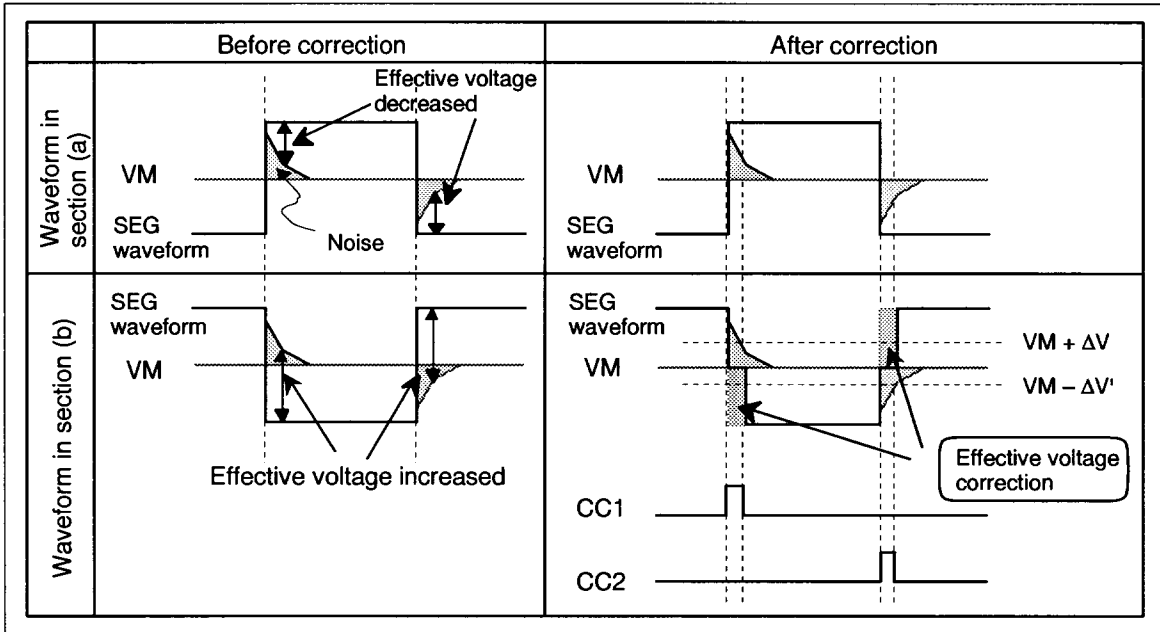


Figure 8 Effective Voltage Correction (1)

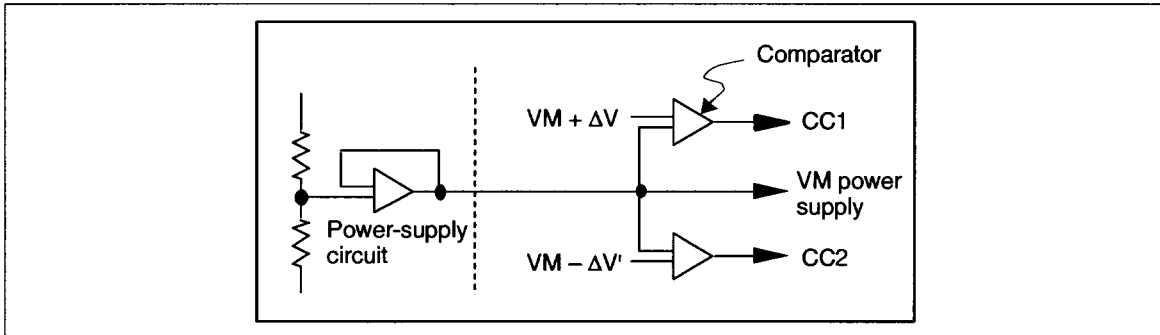


Figure 9 External Circuit Example

(2) CC3 and CC4 (shadowing caused by waveform distortion)

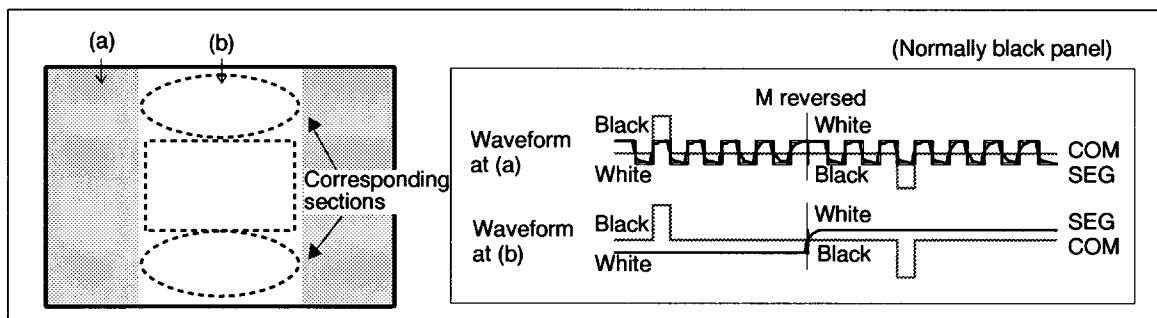


Figure 10 CC3 and CC4

When the background is displayed in grayscale (for example, in a checker pattern), many segment levels are changed in section (a) but not in section (b). The effective voltage for section (a) becomes low because distortion occurs in the segment output waveform due to driver or panel impedance. On the other hand, the effective voltage for section (b) becomes high because the waveform is changed only slightly. Shadowing occurs in the corresponding sections due to the different voltages.

The HD66134STs compare the present output data and the next output data. If the data is not changed, the output level is reset to the VM, which corrects the effective voltages in (a) and (b). The high width is corrected according to the shadowing level for output correction while CC3 and CC4 are high. CC3 corrects the non-selected output pin (black background), and CC4 corrects the selected output pin (white background).

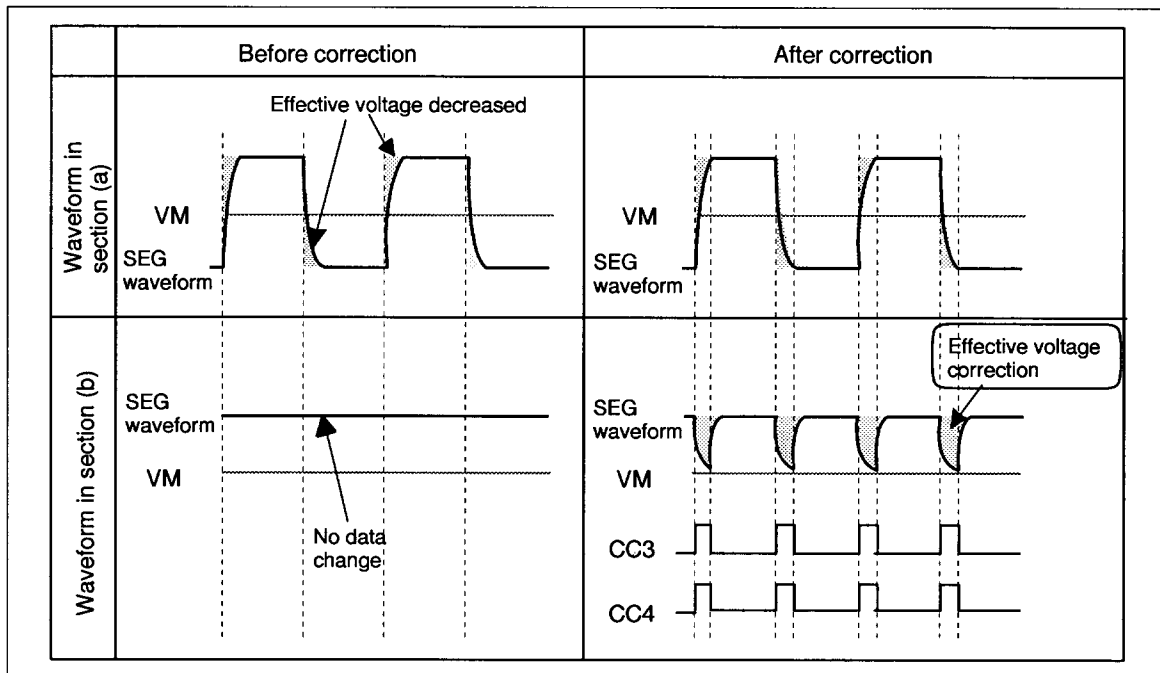


Figure 11 Effective Voltage Correction (2)

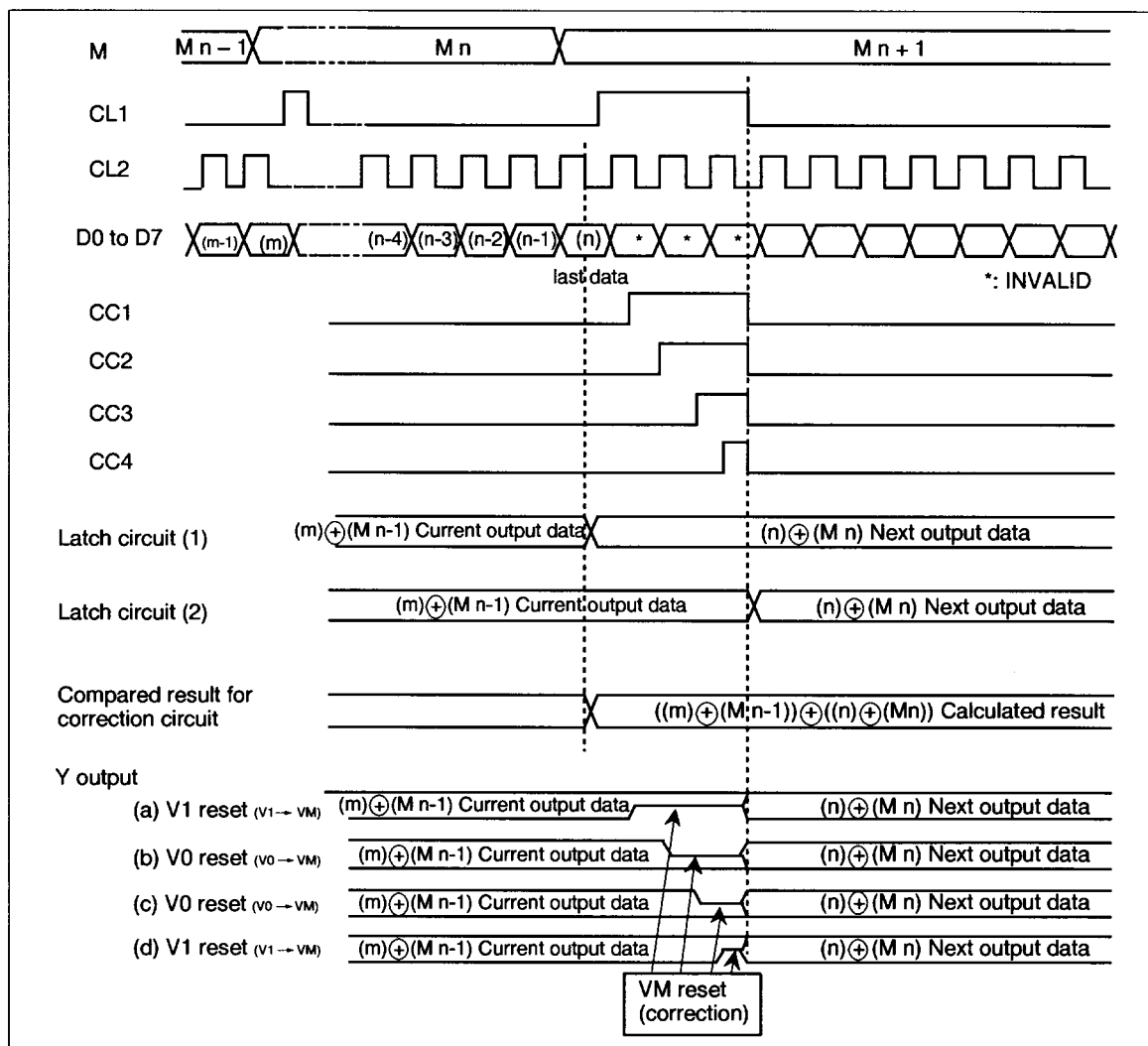


Figure 12 Compared Result for Correction Circuit

The correction circuit compares the present output data (latch circuit (2)) and the next output data (latch circuit (1)). Depending on the compared result, the circuit resets the high width of CC3 to the VM for the output without a data change if the data is the non-selected output ((c) in figure 12). The circuit resets the high width of CC4 to the VM if the data is the selected output ((d) in figure 12). CC3 and CC4 are input after the last valid data is transferred. CC1 forcibly resets the V1 output to VM for the high width ((a) in figure 12). CC2 forcibly resets the V0 output to VM for the high width ((b) in figure 12). Therefore, shadowing caused by waveform distortion is corrected with CC3 or CC4 (non-selected or selected), and shadowing caused by crosstalk is corrected with CC1 or CC2 (in the V0 or V1 direction).

Note: The high period from CC1 to CC4 should be matched with the shadowing level.

Absolute Maximum Ratings*1

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	V_{cc}	-0.3 to +7.0	V	2 and 5
	LCD drive circuit	V0	-0.3 to +7.0	V	2 and 5
Input voltage (1)		VT1	-0.3 to $V_{cc} + 0.3$	V	2 and 3
Input voltage (2)		VT2	-0.3 to $V0 + 0.3$	V	2, 4, and 5
Operating temperature		T_{opr}	-30 to +75	°C	
Storage temperature		T_{stg}	-55 to +110	°C	

- Notes: 1. If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunctions or degraded reliability.
2. The reference point is GND (0 V).
3. Applies to the SHL, $\bar{E}IO1$, $\bar{E}IO2$, DISP, D0 to D7, CL1, CL2, M, and CC1 to CC4 pins.
4. Applies to the VML, VMR, VIL, and VIR pins.
5. As shown in figure 14, users should conform to the following turn-on/off sequence for the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, the LSI reliability will be affected.

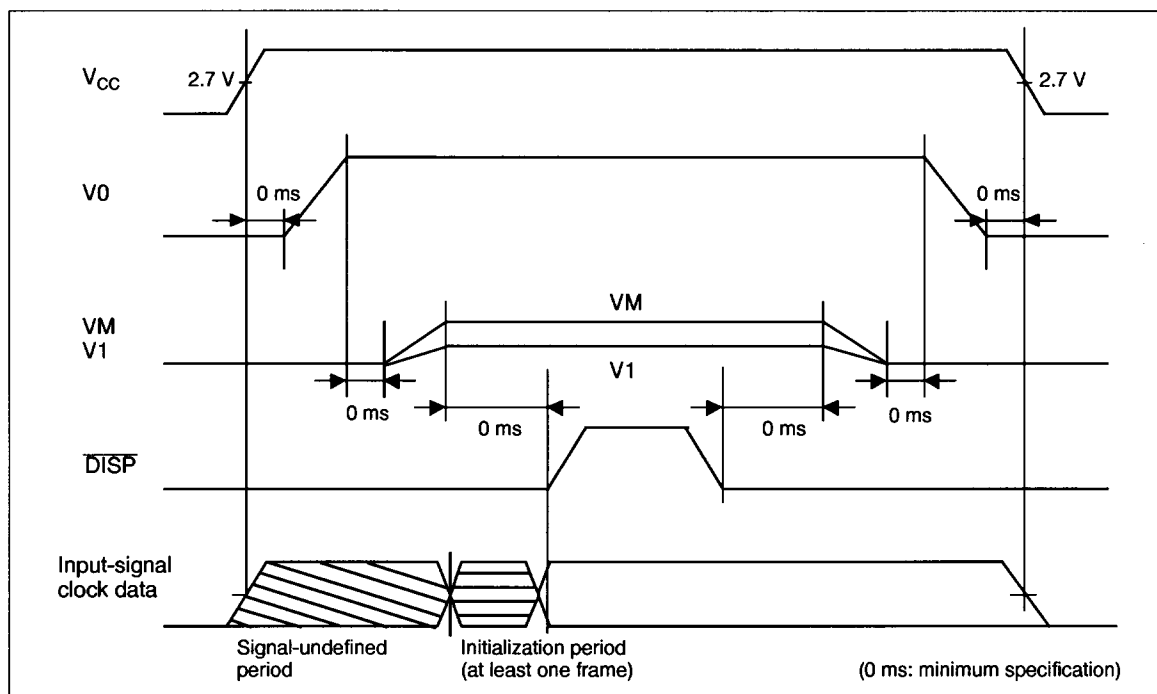


Figure 14 Turn-on and Turn-off Timing

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5.1 Turning on the power

- 1) Turn on the power in the order of GND- V_{CC} , GND-V0, and VM/V1. Then, ground the \overline{DISP} pin.
- 2) The LCD forcibly outputs the VM level by the DISPOFF function.
- 3) Even if an input signal is disturbed immediately after V_{CC} is applied, the DISPOFF function has priority.
- 4) Input the specific signal to initialize the registers in the driver. The initialization period must be at least one frame.
- 5) The preparation for the normal display is completed. Apply the V_{CC} level to the \overline{DISP} pin to cancel the DISPOFF function. At this time, the level of pins V0, VM, and V1 must rise to the specific potential.

5.2 Turning off the power

The procedure is basically the reverse of that used to turn on the power.

- 1) Ground the \overline{DISP} pin.
- 2) Turn off the LCD power in the order of VM/V1 and GND-V0.
- 3) Ground V_{CC} and an input signal.

At this time, the level of pins V0, VM, and V1 must fall to 0 V. Since the DISPOFF function stops when V_{CC} falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

Electrical Characteristics
DC Characteristics 1 ($V_{CC} = 2.7$ to 4.5 V, $V_0-GND = 3.5$ to 5.5 V, and $T_a = -30$ to $+75$ °C)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Notes
Input high-level voltage	V_{IH}	CL1, CL2, SHL, M, EIO1, EIO2, DISP,	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low-level voltage	V_{IL}	D0 to D7, and CC1 to CC4	0	—	$0.3 \times V_{CC}$	V		
Output high-level voltage	V_{OH}	$\overline{EIO1}$ and $\overline{EIO2}$	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4$ mA	
Output low-level voltage	V_{OL}	$\overline{EIO1}$ and $\overline{EIO2}$	—	—	0.4	V	$I_{OL} = 0.4$ mA	
V_i - Y_j ON resistance	RON	Y1 to Y240, V0L, and V0R	—	0.5	1.0	k Ω	$I_{ON} = 150$ μ A	1
		Y1 to Y240, VML, and VMR	—	1.0	2.0	k Ω		
		Y1 to Y240, V1L, and V1R	—	0.5	1.0	k Ω		
Input leakage current (1)	IIL1	CL1, CL2, SHL, M, EIO1, EIO2, DISP, D0 to D7, and CC1 to CC4	-5.0	—	5.0	μ A	$V_{IN} = V_{CC} - GND$	
Input leakage current (2)	IIL2	VML, VMR, V1L, and V1R	-100	—	100	μ A	$V_{IN} = V_0 - GND$	
Current consumption (1)	ICC	V_{CC}	—	1.0	6.0	mA	$V_{CC} = 3.0$ V $f_{CL2} = 25$ MHz	2
Current consumption (2)	IV0	V0L and V0R	—	0.4	1.0	mA	$f_{CL1} = 100$ kHz $f_M = 4$ kHz	
Current consumption (3)	IST	V_{CC}	—	0.4	1.0	mA		2 and 3

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DC Characteristics 2 ($V_{CC} = 4.5$ to 5.5 V, $V_0-GND = 3.5$ to 5.5 V, and $T_a = -30$ to $+75$ °C)

Item	Symbol	Applicable Pin	Min.	Typ.	Max.	Unit	Conditions	Notes
Input high-level voltage	V_{IH}	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$, DISP,	$0.7 \times V_{CC}$	—	V_{CC}	V		
Input low-level voltage	V_{IL}	D0 to D7, and CC1 to CC4	0	—	$0.3 \times V_{CC}$	V		
Output high-level voltage	V_{OH}	$\overline{EIO1}$ and $\overline{EIO2}$	$V_{CC} - 0.4$	—	—	V	$I_{OH} = -0.4$ mA	
Output low-level voltage	V_{OL}	$\overline{EIO1}$ and $\overline{EIO2}$	—	—	0.4	V	$I_{OL} = 0.4$ mA	
V_i - Y_j ON resistance	RON	Y1 to Y240, V0L, and V0R	—	0.5	1.0	k Ω	$I_{ON} = 150$ μ A	1
		Y1 to Y240, VML, and VMR	—	1.0	2.0	k Ω		
		Y1 to Y240, V1L, and V1R	—	0.5	1.0	k Ω		
Input leakage current (1)	IIL1	CL1, CL2, SHL, M, $\overline{EIO1}$, $\overline{EIO2}$, DISP, D0 to D7, and CC1 to CC4	-5.0	—	5.0	μ A	$V_{IN} = V_{CC}-GND$	
Input leakage current (2)	IIL2	VML, VMR, V1L, and V1R	-100	—	100	μ A	$V_{IN} = V_0-GND$	
Current consumption (1)	ICC	V_{CC}	—	3.0	15	mA	$V_{CC} = 5.0$ V $f_{CL2} = 40$ MHz	2
Current consumption (2)	IV0	V0L and V0R	—	0.4	2.0	mA	$f_{CL1} = 160$ kHz $f_M = 6$ kHz	
Current consumption (3)	IST	V_{CC}	—	1.0	2.0	mA		2 and 3

- Notes: 1 Indicates the resistance between one of the pins Y1–Y240 and one of the voltage supply pins, when load current is applied to the Y pin; defined under the following conditions:
 $V_0-GND = 5.5$ V
 $VM = (V_0 + V_1)/2$
 $V_1 = GND + 1$
 V_1 should be near the GND level, and the VM should be near the middle voltage between V_1 and V_0 . V_1 should be within the range of $\Delta V = 0.25 V_0$, which is the range within which RON, the LCD drive circuit's output impedance, is stable. See figure 15.
2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, V_{IH} and V_{IL} must be used at V_{CC} and GND, respectively.
3. Standby current.
4. The voltage of each signal is shown in figure 16.

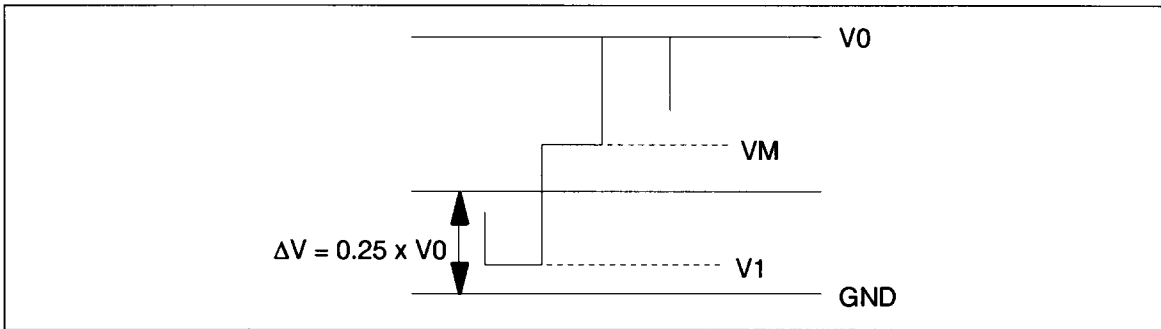


Figure 15 Relationship between Driver-Output Waveforms and Each Level Voltage

Segment voltage	Segment waveform		Common waveform		Common voltage
V0 (5.0 V)					VH (38.0 V)
V _{CC} (3.3 V)					V _{CC} (3.3 V)
VM (3.0 V)					VM (3.0 V)
V1 (1.0 V)					GND (0.0 V)
GND (0.0 V)					GND (0.0 V)
	Normal display period	Display-off period	Normal display period	Display-off period	VL (32.0 V)

Figure 16 Signal Voltages

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AC Characteristics 1 ($V_{CC} = 2.7$ to 4.5 V, $V_0-GND = 3.5$ to 5.5 V, and $T_a = -30$ to $+75$ °C)*1

Item	Symbol	Applicable Pins	Min.	Max.	Unit
Clock cycle time	t_{CYC}	CL2	40	—	ns
Clock high-level width (1)	t_{CWH2}	CL2	15	—	ns
Clock low-level width (1)	t_{CWL2}	CL2	15	—	ns
Clock high-level width (2)	t_{CWH1}	CL1	30	—	ns
Clock setup time	t_{SCL}	CL1 and CL2	20	—	ns
Clock hold time	t_{HCL}	CL1 and CL2	50	—	ns
Clock rise time	t_r	CL1 and CL2	—	30	ns
Clock fall time	t_f	CL1 and CL2	—	30	ns
Data setup time	t_{DS}	D0 to D7, and CL2	10	—	ns
Data hold time	t_{DH}	D0 to D7, and CL2	10	—	ns
M setup time	t_{MS}	M and CL1	20	—	ns
M hold time	t_{MH}	M and CL1	20	—	ns
Output delay time (1)	t_{pd1}	CL1, and Y1 to Y240	—	500	ns
CC setup time	t_{CCS}	CC3 to CC4, and CL1	20	—	ns
CC hold time	t_{CCH}	CC3 to CC4, and CL2	20	—	ns

Note: 1. The load must be less than 10 pF between the $\overline{EIO2}$ and $\overline{EIO1}$ connections of the HD66134STs.

AC Characteristics 2 ($V_{CC} = 4.5$ to 5.5 V, $V_0-GND = 3.5$ to 5.5 V, and $T_a = -30$ to $+75$ °C)*1

Item	Symbol	Applicable Pins	Min.	Max.	Unit
Clock cycle time	t_{cyc}	CL2	25	—	ns
Clock high-level width (1)	t_{cwh2}	CL2	10	—	ns
Clock low-level width (1)	t_{cwl2}	CL2	10	—	ns
Clock high-level width (2)	t_{cwh1}	CL1	25	—	ns
Clock setup time	t_{scl}	CL1 and CL2	20	—	ns
Clock hold time	t_{hcl}	CL1 and CL2	50	—	ns
Clock rise time	t_r	CL1 and CL2	—	20	ns
Clock fall time	t_f	CL1 and CL2	—	20	ns
Data setup time	t_{ds}	D0 to D7, and CL2	6	—	ns
Data hold time	t_{dh}	D0 to D7, and CL2	6	—	ns
M setup time	t_{ms}	M and CL1	20	—	ns
M hold time	t_{mh}	M and CL1	20	—	ns
Output delay time (1)	t_{pd1}	CL1, and Y1 to Y240	—	500	ns
CC setup time	t_{ccs}	CC3 to CC4, and CL1	20	—	ns
CC hold time	t_{cch}	CC3 to CC4, and CL2	20	—	ns

- Notes: 1. The load must be less than 10 pF between the $\overline{EIO2}$ and $\overline{EIO1}$ connections of the HD66134STs.
 2. For output delay time 1, connect the load circuit as shown in figure 17.

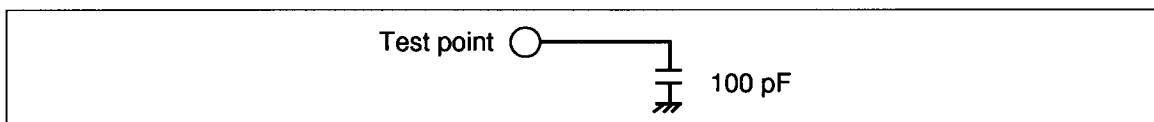


Figure 17 Load Circuit for Output Delay Time 1

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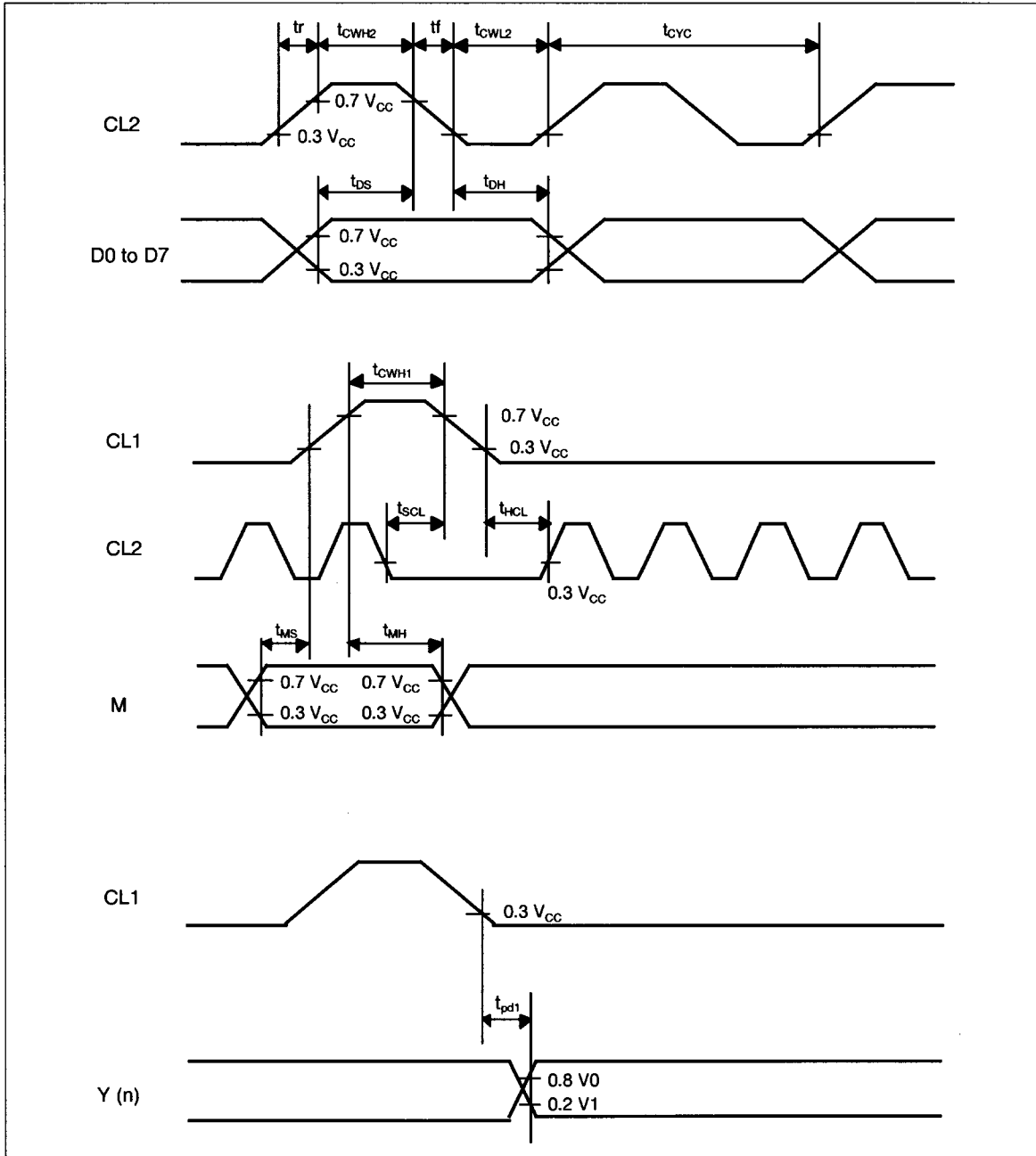


Figure 18 AC Characteristics (1)

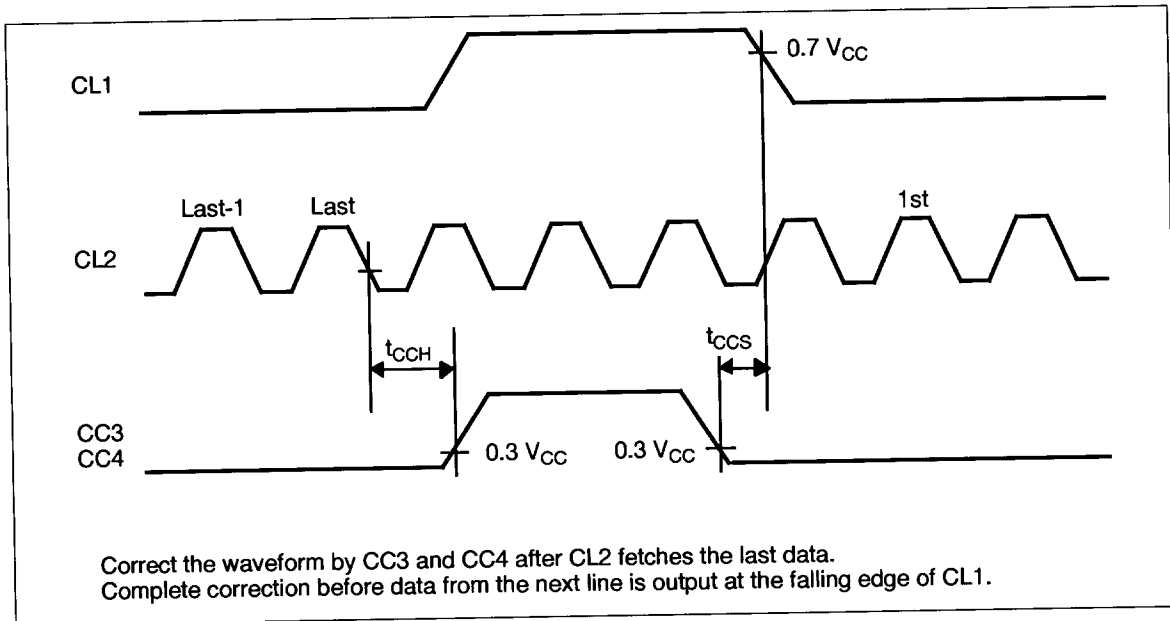


Figure 19 AC Characteristics (2)