
HD66135T

120-Channel High-Voltage Common Driver for a Dot-Matrix STN
Liquid Crystal Display

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Rev 1
Nov. 27, 1996

Description

The HD66135T is a 120-channel common driver for driving a dot-matrix STN liquid crystal display (LCD) panel. Since the driver uses a high-voltage (75 V) process, the operating voltage from -37.5 to +37.5 V is enabled with level VM in the center. It operates at a low logic drive voltage of 3 V. This driver is used together with segment driver HD66134T, which is built into the shadowing correction circuit.

Features

- Duty cycle: Up to 1/300
- LCD drive voltage: 75 V
- Number of LCD drive circuits: 120 circuits
- Operating voltage: 2.7 to 5.5 V
- Output division function (60 × 2 outputs)
- Display-off function
- Slim tape-carrier package (TCP)
 - Output lead pitch: 190 μm
 - User area: 10.5 mm
- Low output impedance: 0.5 kΩ (typ)
- Intermediate voltage I/F

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Pin Arrangement

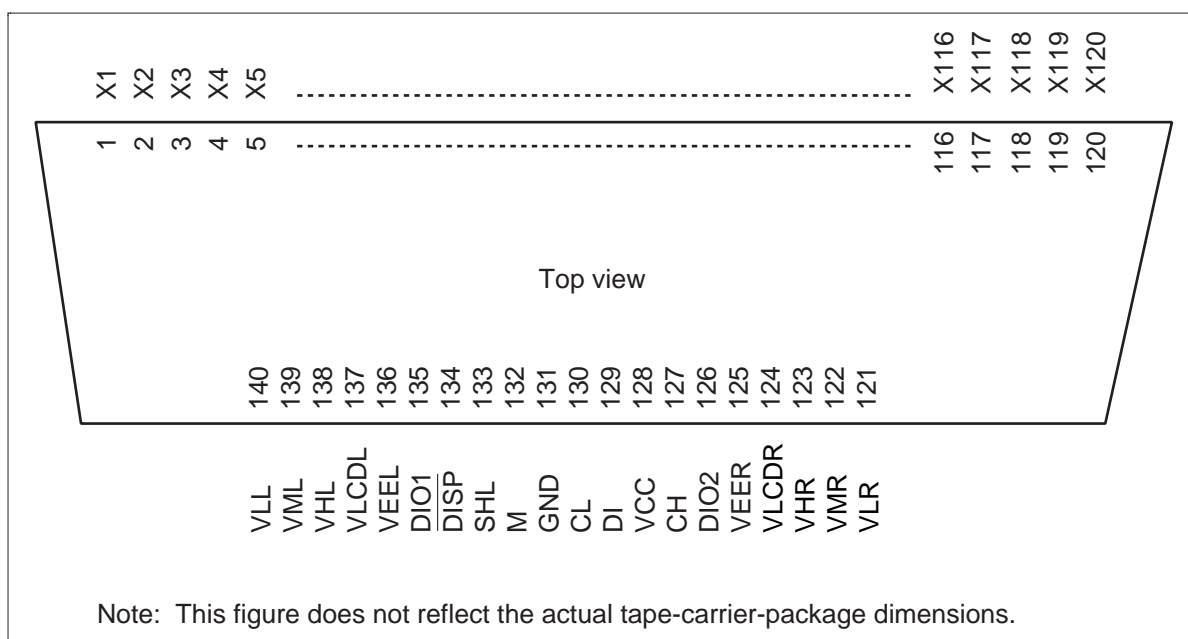


Figure 1 Pin Arrangement

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Block Diagram

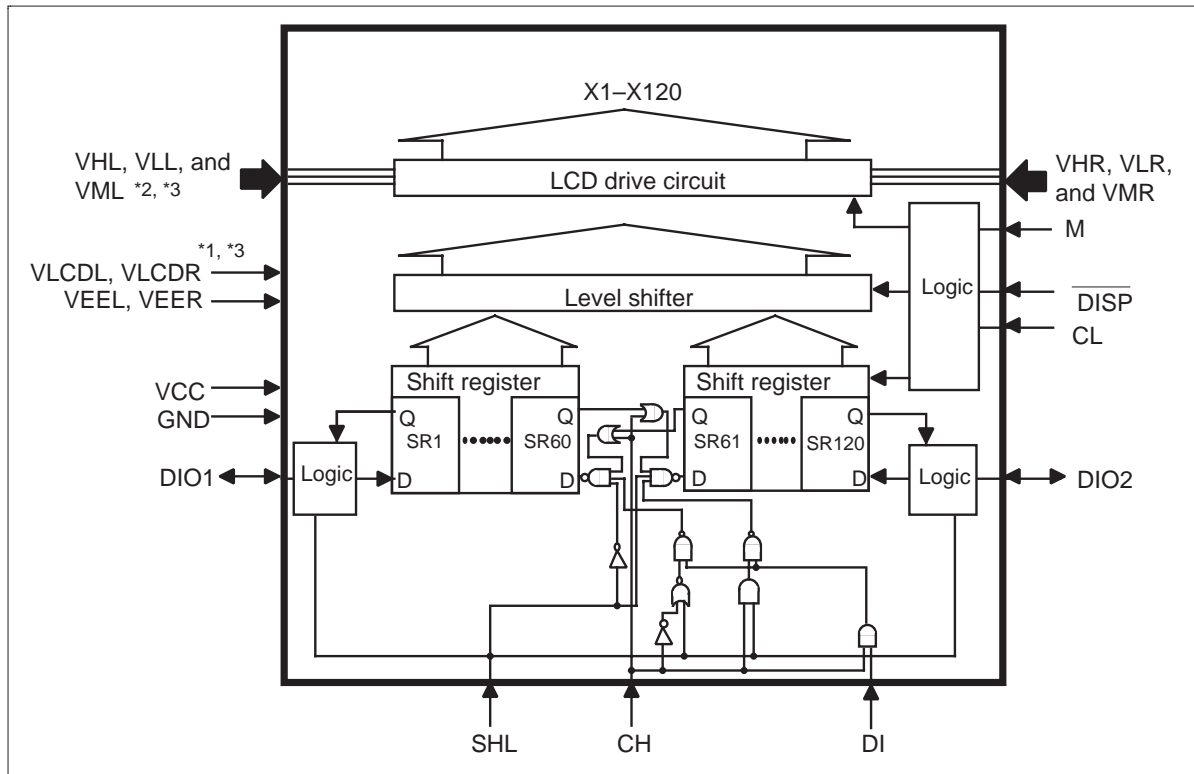


Figure 2 Block Diagram

- Notes:
1. VLCDL and VEEL are internally connected to VLCDR and VEER, respectively.
 2. VHL, VLL, and VML are internally connected to VHR, VLR, and VMR, respectively.
 3. VLCDL and VLCDR are internally connected to VHL and VHR, respectively, and VEEL and VEER are internally connected to VLL and VLR, respectively.

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Block Functions

LCD Drive Circuit

The 120-bit LCD drive circuit generates three voltage levels V_H , V_L , and V_M , which drive the LCD panel. One of these three levels is output to the corresponding X pin, depending on the combination of the M signal and the data in the shift register.

Level Shifter

The level shifter changes the logic control signals (5 V) into high-voltage signals for the LCD drive circuit.

Shift Register

The 120-bit shift register shifts the data input via the DIO pin with shift clock CL. The SHL pin selects the data-shift direction.

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Pin Functions

Table 1 Pin Functions

Classification	Symbol	Pin No.	Pin Name	Input/ Output	Function	
Power supply	VLCDL	137	VLCDL	—	VLCDL, VLCDR–VEEL, VEER: LCD drive power supply VCC–GND: Logic power supply	
	VLCDR	124	VLCDR			
	VEEL	136	VEEL			
	VEER	125	VEER			
	VCC	128	VCC			
	GND	131	GND			
		VHL	138	VHL	Input	LCD drive voltage level
		VHR	123	VHR		VHL, VHR: Selection level (equivalent to VLCDL and VLCDR levels)
		VLL	140	VLL		VLL, VLR: Selection level (equivalent to VEEL and VEER levels)
		VLR	121	VLR		VML, VMR: Non-selection level
Control signal	CL	130	Clock	Input	Inputs data shift clock pulses for the shift register. At the falling edge of each CL pulse, the shift register shifts the data input.	
	M	132	M	Input	Changes the LCD drive outputs to AC.	
	CH	127	CH	Input	Selects the data-shift mode. (CH = low: 120-output mode, CH = high: 60 × 2-output mode)	
	SHL	133	Shift left	Input	Selects the data-shift direction as shown in Table 2.	
	DIO1	135	Data	Input/ output	Serial input/output (shift-register-data input/output). This pin is used for serial input when SHL is high, and for serial output when SHL is low.	
	DIO2	126	Data	Input/ output	Serial input/output (shift-register-data input/output). This pin is used for serial input when SHL is low, and for serial output when SHL is high.	
	DI	129	Data	Input	Serial input (shift-register-data input). In the 60 × 2-output mode, shift register data is input to pins X61 to X120 in serial when SHL is high, and to pins X1 to X60 in serial when SHL is low. This pin must be connected to GND when not used.	
	DISP	134	Disp off	Input	Pins X1 to X120 are set at level VM by connecting this pin to GND. Registers are not cleared.	
LCD drive output	X1 to X120	1 to 120	X1 to X120	Output	One of three levels VH, VL, and VM is output according to the combination of the M signal and display data when the DISP pin is connected to VCC. See figure 3.	

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Table 2 Shift Direction of the Shift Register

SHL	Data-Shift Direction
High	Shift to right DIO1 → SR1 → SR2.....SR120 → DIO2
Low	Shift to left DIO2 → SR120 → SR119.....SR1 → DIO1

Note: SR1 to SR120 correspond to the outputs of X1 to X120, respectively.

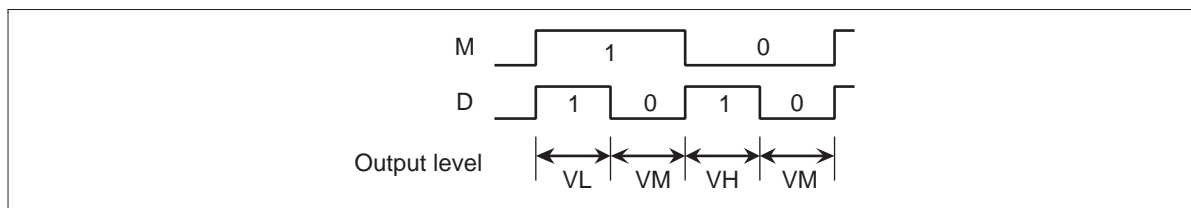


Figure 3 Selection of the LCD Drive Output Level

Absolute Maximum Ratings^{*1}

Item	Symbol	Ratings	Unit	Notes	
Power supply voltage	Logic circuit	VCC	-0.3 to +7.0	V	2 and 7
	LCD drive circuit	VLCD	-0.3 to +41	V	2 and 7
		VEE	-39 to +0.3	V	2 and 7
Input voltage (1)	VT1	-0.3 to VCC + 0.3	V	2 and 3	
Input voltage (2)	VH	= VLCD	V	4	
Input voltage (3)	VL	= VEE	V	5	
Input voltage (4)	VM	- 5.0 to + 10.0	V	6 and 7	
Operating temperature	Topr	-20 to +75	°C		
Storage temperature	Tstg	-40 to +125	°C		

Notes: 1 If the LSI is used beyond these maximum ratings, it will be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunctions or degraded reliability.

2. The reference point is GND (0 V).
3. Applies to the CL, M, SHL, DI, DISP, CH, DIO1, and DIO2 pins.
4. Applies to the VHL and VHR pins.
5. Applies to the VLL and VLR pins.
6. Applies to the VML and VMR pins.
7. Conform to the following turn-on/off sequence of the power and signals. Otherwise, the LSI will malfunction or will be permanently damaged. In addition, the LSI reliability will be affected.

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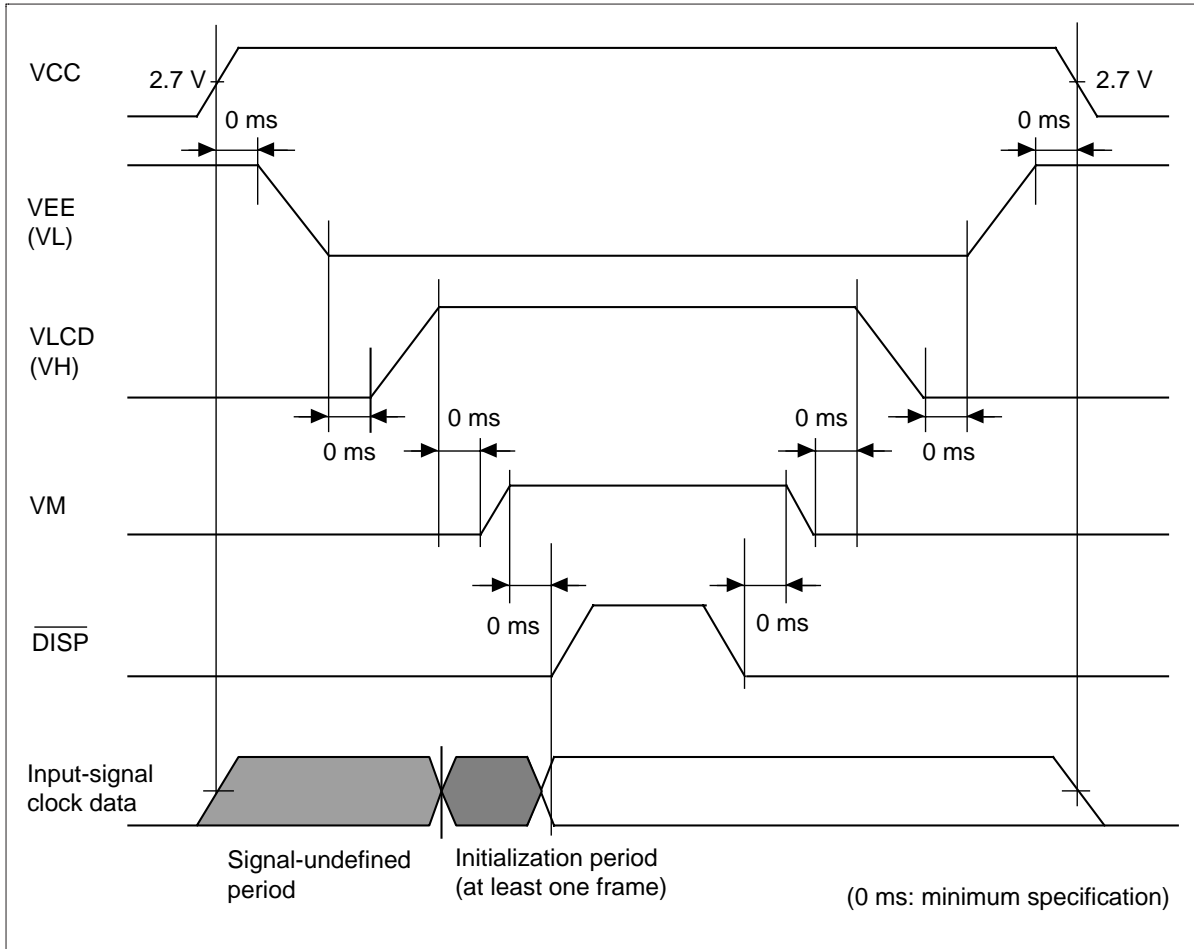


Figure 4 Power and Signal Sequence

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7.1 Turning on the power

- 1) Turn on the power in the order of GND-VCC, GND-VEE (VL), GND-VLCD (VH), and VM. Then, ground the `DISP` pin.
- 2) The LCD forcibly outputs the VM level by the DISPOFF function.
- 3) Even if an input signal is disturbed immediately after VCC is applied, the DISPOFF function has priority.
- 4) Input the appropriate signal to initialize the registers in the driver. The initialization period must be at least one frame.
- 5) The preparation for normal display is completed. Apply the VCC level to the `DISP` pin to cancel the DISPOFF function. At this time, the level of pins VEE (VL), VLCD (VH), and VM must rise to the appropriate potential.

7.2 Turning off the power

The procedure is basically the reverse of that for turning on the power.

- 1) Ground the `DISP` pin.
- 2) Turn off the LCD power in the order of VM, GND-VLCD (VH), and GND-VEE (VL).
- 3) Ground VCC and the input signal.

At this time, the level of pins VEE (VL), VLCD (VH), and VM must fall to 0 V. Since the DISPOFF function stops when VCC falls to 0 V, the LCD may output a level other than VM. Therefore, a display failure may occur when the power is turned off or on.

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Electrical Characteristics

DC Characteristics (VCC = 2.7 to 5.5 V, GND = 0 V, VLCD – VEE = 40 to 75 V, and Ta = –20 to +75 °C, unless otherwise stated)

Item	Symbol	Applicable Pins	Min.	Typ.	Max.	Unit	Conditions	Note
Input high-level voltage	ViH	CL, M, SHL, CH, DI, DIO1, DIO2,	0.7 × VC C	—	VCC	V		
Input low-level voltage	ViL	and DISP	0	—	0.3 × VC C	V		
Output high-level voltage	VOH	DIO1 and DIO2	VCC –0.4	—	—	V	IOH = –0.4 mA	
Output low-level voltage	VOL	DIO1 and DIO2	—	—	0.4	V	IOL = 0.4 mA	
Vi–Xj ON resistance	RON	X1 to X120, and V	—	0.5	0.7	kΩ	ION = 150 μA	1
Input leakage current (1)	IiL1	CL, M, SHL, CH, DI, DIO1, DIO2, and DISP	–5	—	5	μA	VIN = VCC to GND	
Input leakage current (2)	IiL2	VH, VL, and VM	–25	—	25	μA		
Current consumption	ICC	VCC	TBD	TBD	TBD	mA	fCL = 160 kHz fM = 6 kHz	2
Current consumption	ILCD	VLCD	TBD	TBD	TBD	mA		

- Notes: 1. The resistance between the X pin and the V pin (one of the voltage supply pins VH, VL, and VM), when a load current is applied to one of the pins from X1 to X120; defined under the following conditions:
 VLCD = VH = 36 V, VEE = VL = –30 V, VM = 3 V, and GND = 0 V.
 The VH, VL, and VM voltages must be within VLCD = VH = 40.5 to 23 V, VEE = VL = –34.5 to –17 V, and 9 V > VM > –4 V.
2. Input and output currents are excluded. When a CMOS input is left floating, excess current flows from the power supply through the input circuit. To avoid this, ViH and ViL must be held at VCC and GND, respectively.
3. The voltage of each signal is shown in figure 5.

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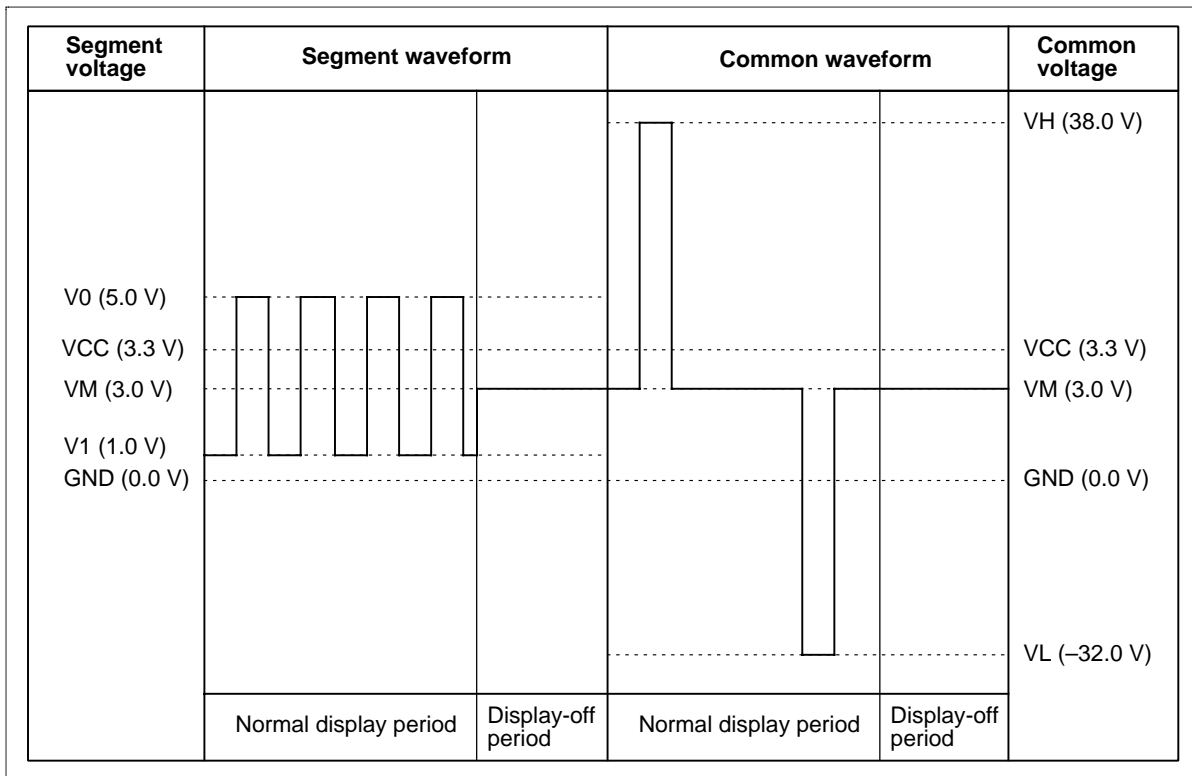


Figure 5 Signal Voltages

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AC Characteristics (1) (VCC = 2.7 to 4.5 V, GND = 0 V, VLCD – VEE = 40 to 75 V, and Ta = –20 to +75 °C)

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	tCYC	CL	400	—	ns	
Clock high level width	tCWH	CL	40	—	ns	
Clock low level width	tCWL	CL	370	—	ns	
Clock rise time	tr	CL	—	30	ns	
Clock fall time	tf	CL	—	30	ns	
Data setup time	tDS	DI, DIO1, DIO2, and CL	100	—	ns	
Data hold time	tDH	DI, DIO1, DIO2, and CL	30	—	ns	
Data output delay time	tDD	DIO1, DIO2, and CL	—	350	ns	1
M setup time	tMS	CL and M	20	—	ns	
M hold time	tMH	CL and M	20	—	ns	
Output delay time (1)	tpd1	X (n) and CL	—	1.2	µs	2

Notes: 1. Defined by connecting the load circuit shown in figure 6.
2. Defined by connecting the load circuit shown in figure 6.

AC Characteristics (2) (VCC = 4.5 to 5.5 V, GND = 0 V, VLCD – VEE = 40 to 75 V, and Ta = –20 to +75 °C)

Item	Symbol	Applicable Pins	Min.	Max.	Unit	Note
Clock cycle time	tCYC	CL	400	—	ns	
Clock high level width	tCWH	CL	25	—	ns	
Clock low level width	tCWL	CL	370	—	ns	
Clock rise time	tr	CL	—	30	ns	
Clock fall time	tf	CL	—	30	ns	
Data setup time	tDS	DI, DIO1, DIO2, and CL	100	—	ns	
Data hold time	tDH	DI, DIO1, DIO2, and CL	30	—	ns	
Data output delay time	tDD	DIO1, DIO2, and CL	—	150	ns	1
M setup time	tMS	CL and M	20	—	ns	
M hold time	tMH	CL and M	20	—	ns	
Output delay time (1)	tpd1	X (n) and CL	—	0.7	µs	2

Notes: 1. Defined by connecting the load circuit shown in figure 6.
2. Defined by connecting the load circuit shown in figure 6.

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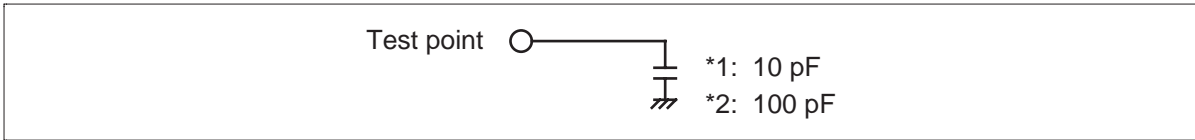


Figure 6 Load Circuit

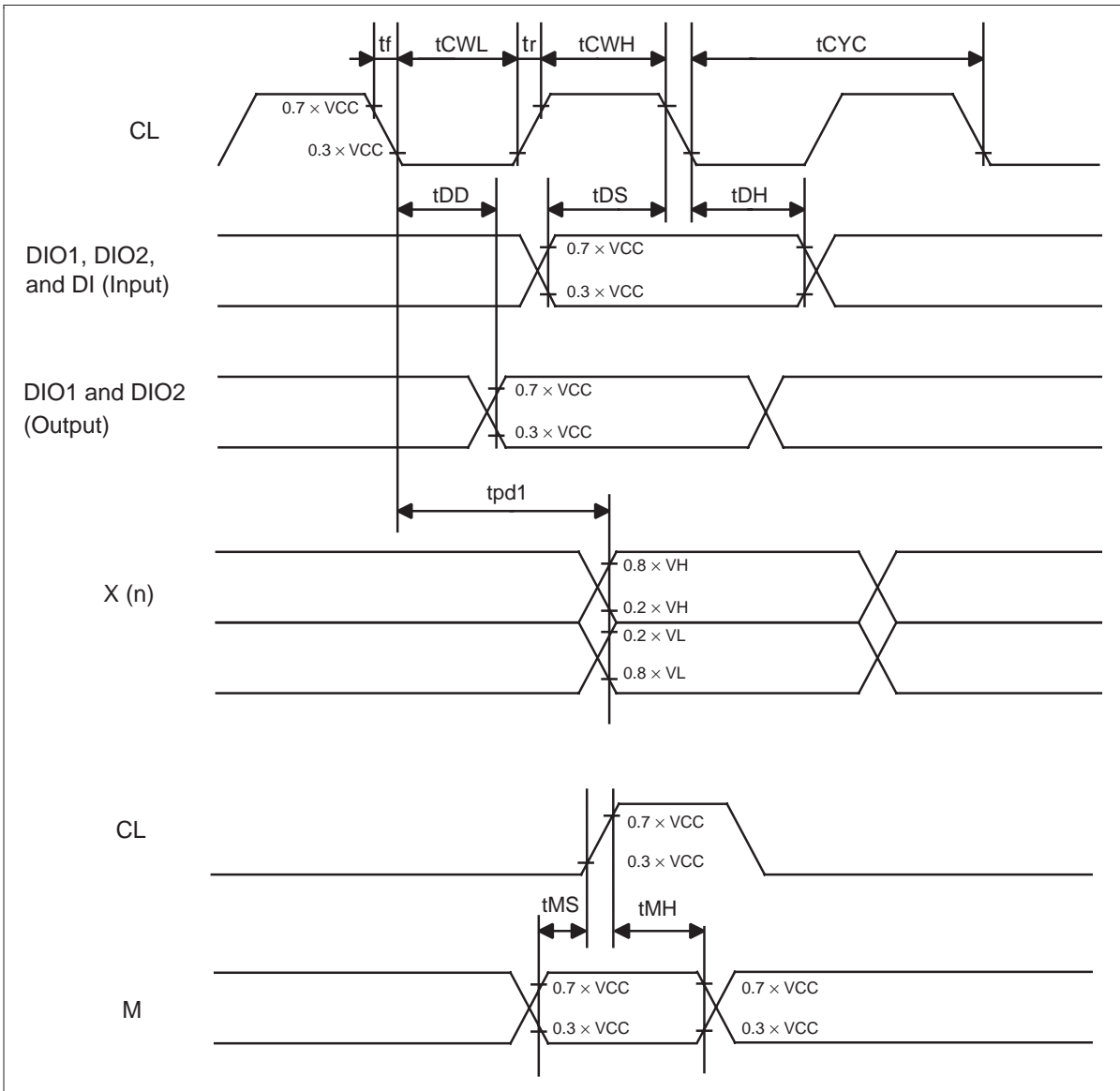


Figure 7 AC Characteristics

