HD66522

(160-Channel Column Driver with Internal Bit-Map RAM for Reflective Color Display and Grayscale Display)

HITACHI

Preliminary

Description

The HD66522 is a column driver for liquid crystal dot-matrix graphic display system. This LSI incorporates 160 liquid crystal drive circuit and a 160 * 240 * 2-bit bit-mapped RAM, which is suitable for LCDs in portable information devices. It also includes a general-purpose SRAM interface so that draw access can be easily implemented from a general-purpose MPU. The HD66522 also has a new arbitration method which prevents flicker when the MPU performs draw access asynchronously. The on-chip display RAM greatly decreases power consumption compared to previous liquid crystal display system because there is no need for high speed data transfer. The chip also incorporates a four-level grayscale out of 32-level grayscale palette controller for enhanced graphics capabilities and reflective color.

Features

- Duty cycle: 1/64 to 1/240
- Liquid crystal drive circuits: 160
- Logic circuit: 2.4 to 3.6V
- Liquid crystal drive circuit: 4 to 6V
- LCD driving technique: Multi-line addressing
- Grayscale display: FRC four-level grayscale out of 32 levels grayscale palette
- Grayscale memory management: Packed pixel
- Internal bit-map display memory: 76800 bits (160 * 240 lines * two planes)
- MPU interface

  SRAM interface

  Address bus: 16 bits

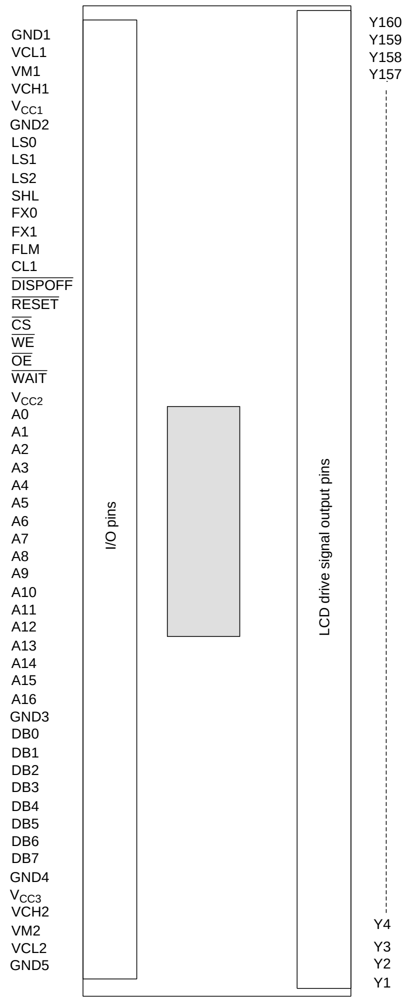
  Data bus: 8 bits

- High-speed draw function: Supports burst transfer mode
- Arbitration function: Implemented internally (draw access has priority)
- Access time: 120ns
- Low power consumption
- On-chip address management function
- Refresh unnecessary
- Internal display off function
- Package: TCP or die with gold bump

Orderling Information

Type No.	Package	Outer Lead Pitch (μm)
HD66522TA0	213 pin TCP	200
HCD66522BP	Die with gold bump	—

Pin Arrangement



Note: This figure is not drawn to a scale.

Pin Description

Classi-fication	Symbol	Pin Name	I/O	Number of Pins	Function
Power supply	V_{CC1}, V_{CC2} V_{CC3}	V_{CC}	—	3	V_{CC}–GND: logic power supply
	GND1 to GND5	GND	—	5	Ground
	VCH1 VCH2	Column drive selecet high-level	—	2	VCH–GND: LCD drive circuit power supply and LCD drive level power supplies
	VM1 VM2	LCD deselect mid-level voltage	—	2	LCD drive level power supplies See Figure 1. The same level must be supplied to both pins.
	VCL1 VCL2	Column drive selecet low-level	—	2	LCD Column drive selects low-level
Control signals	LS0 LS1 LS2	LSI ID select switch pin 0,1 and 2	I	3	Pins for setting LSI ID No (refer to **Pin functions** for details).
	SHL	Shift direction control signal	I	1	Reverses the relationship between LCD drive output pins Y and addresses.
	FLM	First line marker	I	1	First line select signal.
	CL1	Data transfer clock	I	1	Clock signal to transfer the line data to an LCD display driver block.
	FX0 FX1	Scan function data	I	2	Scan function data to select LCD driver output level
	$\overline{\text{DISPOFF}}$	Display off signal	I	1	Control signal to fix LCD driver outputs to LCD deselect mid level. When low, LCD drive outputs Y1 to Y160 are set to VM. Display can be turned off by setting a common driver to VM.
	$\overline{\text{RESET}}$	Reset	I	1	Setting this pin low initializes the HD66522
Bus inter-face	A0 to A16	Address input	I	17	Upper 9 bits (A16–A8) are used for the duty-directional addresses, and lower 8 bits (A7–A0) for the output-pin directional addresses (refer to **Pin Functions** for details).
	DB0 to DB7	Data input/output	I/O	8	Packed-pixel 2-bit/pixel display data transfer (refer to **Pin Functions** for details).
	$\overline{\text{CS}}$	Chip select signal	I	1	LSI select signal during draw access (refer to **Pin Functions** for details).
	$\overline{\text{WE}}$	Write signal	I	1	Write-enable signal during draw access (refer to **Pin Functions** for details).
	$\overline{\text{OE}}$	Output Enable signal	I	1	Output-enable signal during draw access (refer to **Pin Functions** for details).
	$\overline{\text{WAIT}}$	Wait signal	O	1	Status output signal
LCD drive output	Y1 to Y160	LCD drive output	O	160	Each Y outputs one of the three voltage levels VCH, VM or VCL, depending on the combination of the FX0 or FX1 signal and data levels.

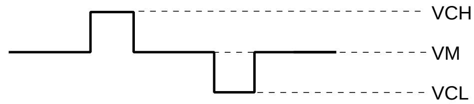


Figure 1   LCD Drive Levels

Pin Functions

Power Supply Pins

V_{CC1} to V_{CC3}, GND1 to GND5: These pins supply power to the logic circuit.

VCH1 and VCH2: These pins supply power to the liquid crystal circuits and level supplies for LCD driver. The same voltage must be supplied.

VM1, VM2, VCL1, VCL2: These Pins input the level supply for LCD driver. The same voltage must be supplied to VM1 and VM2, VCL1 and VCL2.

Control Signals

LS0, LS1 and LS2 (Input): The LS pins can assign eight (0 to 7) ID numbers to eight LSIs, thus making it possible to connect a maximum of eight HD66522s sharing the same CS pin to the same bus (Figure 2).

SHL (Input): This pin reserves the relationship between LCD drive output pins Y1 to Y160 and addresses. There is no need to change the addresses assignment for the display regardless of whether the HD66522 is mounted from the back or the front of the LCD panel. Refer to Driver Layout and Address Management for details.

FLM (Input): When the pin is high, it resets the display line counter, returns the display line to the start line, and synchronizes common signals with frame timing.

CL1 (Input): At each falling edge of data-transfer clock pulses input to this pin, the latch circuits latch display data and output it to the liquid crystal display driver section.

FX0 and FX1 (Input): Scanning function data signal to select LCD driver output. Connect with FX0, FX1 pins of common driver HD66523.

$\overline{\text{DISPOFF}}$ (Input): A control signal to fix liquid crystal driver output to liquid crystal deselect level. When this pin is low, liquid crystal drive outputs Y1 to Y160 are set to liquid crystal deselect level VM. The display can be turned off by setting the outputs of the common driver to level VM. In this case, display RAM data will be retained. Therefore, if signal $\overline{\text{DISPOFF}}$ returns to high level, liquid crystal drive outputs will return to normal display state. Draw access can be executed when signal $\overline{\text{DISPOFF}}$ is either in high or low state.

$\overline{\text{RESET}}$ (Input): Low level of $\overline{\text{RESET}}$ stops internal operation and initializes internal registers and counters.

Bus Interface

$\overline{\text{CS}}$ (Input): A basic signal of the RAM area. When $\overline{\text{CS}}$ is low (active), the system can access the on-chip RAM of the LSI whose address space, set by LS0, LS1, LS2 and SHL pins, contains the input address. When $\overline{\text{CS}}$ is high, the draw access is disabled.

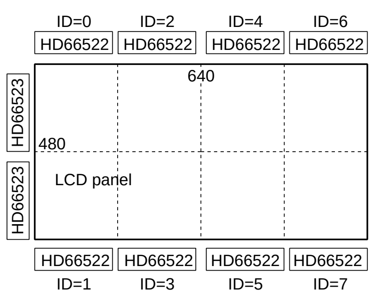
A0 to A16 (Input): A bus to transfer addresses during RAM access. Upper nine bits (A16 to A8) are duty-direction addresses, and lower eight bits (A7 to A0) are output pin-direction addresses.

$\overline{\text{WAIT}}$ (Output): This signal outputs low during display access. The CPU must wait finishing the bus cycle until this signal goes high. The $\overline{\text{WAIT}}$ is in high-impedance condition while $\overline{\text{CS}}$ is high, so this pin must be pulled-up with a resistor outside of the HD66522.

$\overline{\text{WE}}$ (Input): The CPU can write display data to the internal RAM while $\overline{\text{WE}}$ is low. Only the LSI whose address space, set by pins LS0, LS1, LS2 and SHL, contains the input address can be written to when $\overline{\text{CS}}$ is low.

$\overline{\text{OE}}$ (Input): The CPU can read display data from the internal RAM while $\overline{\text{OE}}$ is low. Only the LSI whose address space, set by pins LS0, LS1, LS2 and SHL, contains the input address can be read from when $\overline{\text{CS}}$ is low.

DB7 to DB0 (Input/Output): The pin function as data input/output pins. They can accomodate to a data format with 2 bits/pixcel, which implement packed-pixcel four-level grayscale display.



LS2	LS1	LS0	ID No.	RAM Address Arrangement
L	L	L	0	Upper-side Left to Right
L	H	L	2	
H	L	L	4	
H	H	L	6	
L	L	H	1	Lower-side Left to Right
L	H	H	3	
H	L	H	5	
H	H	H	7	

L: Low Level H: High Level

Figure 2 LS Pins and Address Assignment

Block Diagram

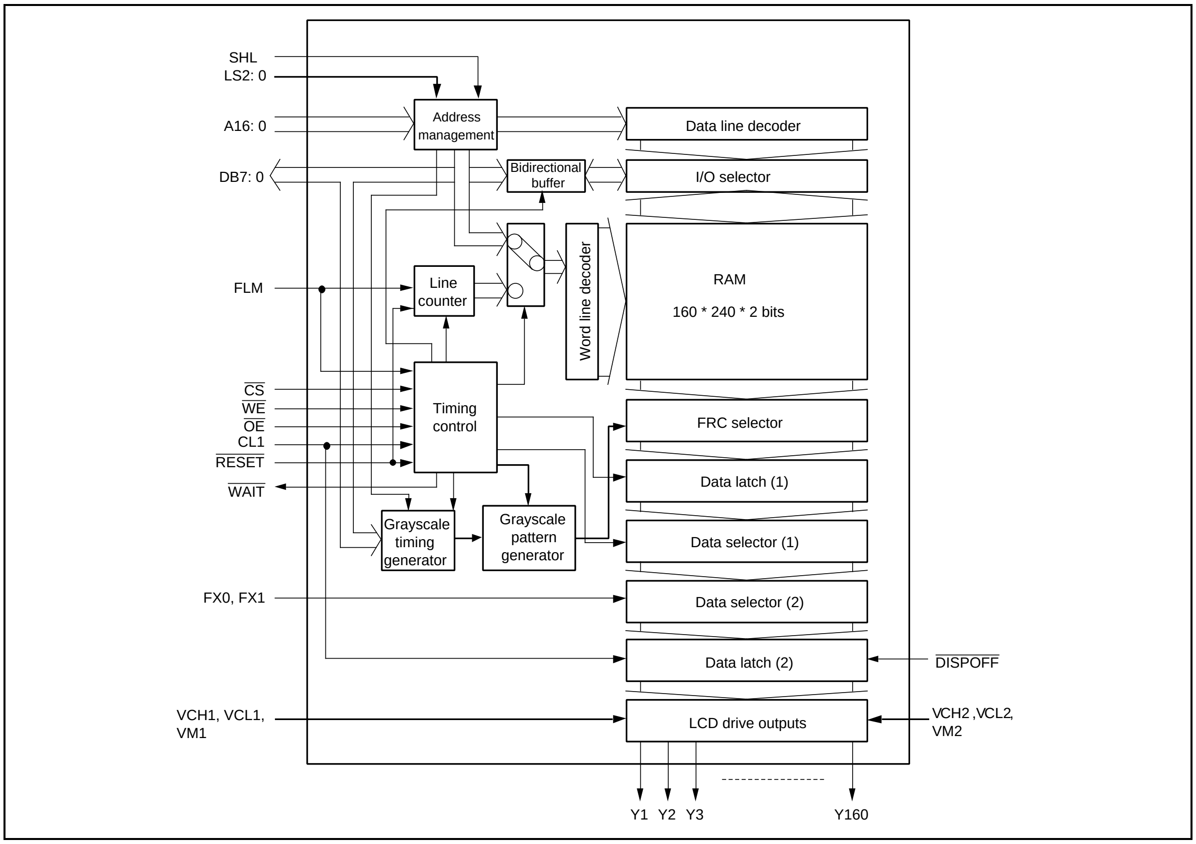


Figure 3 Block Dipagram

Block Diagram

Timing Control Circuit: This circuit controls arbitration between display access and draw access. Specifically, it controls access timing while receiving signals FLM, CL1, $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$ as input. FLM and CL1 are used to perform refresh (display access), that is, to transfer line data to the liquid crystal circuit. $\overline{CS}$, $\overline{WE}$ and $\overline{OE}$ are used for the CPU to perform draw operation (draw access), that is, to read and write display data from and the internal RAM. This circuit also generates a timing signal for the FRC control circuit to implement four-level grayscale display.

Bidirectional Buffer: Controls the transfer direction of the display data according to signals from pins $\overline{WE}$ and $\overline{OE}$ in draw operation from the system.

Word Line Decoder: Decodes duty addresses (A16 to A8) and selects one of 240 lines in the display RAM section, and activates one-line memory cells in the display RAM section.

Data Line Decoder: Decodes pin addresses (A7 to A0) and selects a data line in the display RAM section for the 8-bit memory cells in one-line memory cells activated by the word line decoder.

I/O selector: Reads and writes 8-bit display data for the memory cells in the RAM section.

Display RAM: 160 * 240 * 2-bit memory cell array. Since the memory is static, display data can be held without refresh operation during power supply.

FRC Circuit: Implements FRC (frame rate control) function for four-level grayscale display. For details, refer to **Half Tone Display**.

Data Latch Circuit (1): Latches 160-pixel grayscale display data processed by the FRC control circuit after being read from the display RAM section by refresh operation. This circuit is needed to arbitrate between display access for performing liquid crystal display and draw access from the CPU.

Data Selector (1): This circuit selects data from data latch circuit (1).

Data Selector (2): The display data is generated according to the scanning function signal, FX1 and FX0, and data from data selector (1).

Data Latch Circuit (2): This circuit again latches the data from data selector (2) synchronously with signal CL1.

LCD Drive Circuit: Selects one of LCD select/deselect power levels VCH, VM and VCL according to the grayscale display data, line number, frame number and display-off signal $\overline{DISPOFF}$. The circuits are configurated with 160 circuits each generating LCD voltage to turn on/off the display.

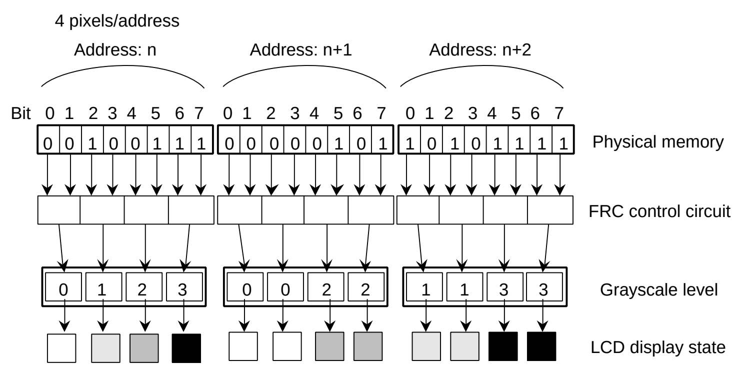
Configuration of Display Data Bit

Packed Pixel Method

For grayscale display, multiple bits are needed for one pixel. In the HD66522, two bits are assigned to one pixel, enabling a four-level grayscale display.

One address (eight bits) specifies four pixels, and pixel bits 0 and 1 are managed as consecutive bits. When grayscale display data is manipulated in bit units, one memory access is sufficient, which enables smooth high-speed data rewriting.

The bit data to input to pin DB7, DB5, DB3 and DB1 become MSB and the bit data to input via pin DB6, DB4, DB2 and DB0 are LSB.



Note: Black is shown when the voltage which exceed threshold voltage is supplied and white is shown when the voltage which is under threshold voltage is supplied at default condition

Figure 4 Packed Pixel System

Half Tone Display (FRC: Frame Rate Control Function)

The HD66522 incorporates an FRC function to display four-level grayscale half tone. Since the HD66522 contains 32-level tone to drive reflective colour liquid crystal, four-level would be selected which adapt to the using liquid crystal.

The FRC function utilizes liquid crystal characteristics whose transmittance is changed by an effective value of applied voltage.

Half tone or reflective colour liquid crystal is expressed in addition to display on/off.

Since the HD66522 has two-bit grayscale data per one pixel, it can display four level grayscale or four-colour and improve user interface (Figure 5). Figure 6 shows the relationships between the effective voltage value and transmittance.

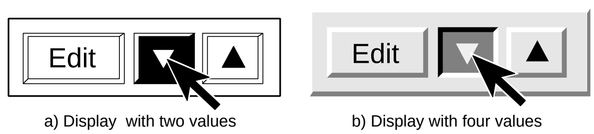


Figure 5 Example of User Interface Improvement

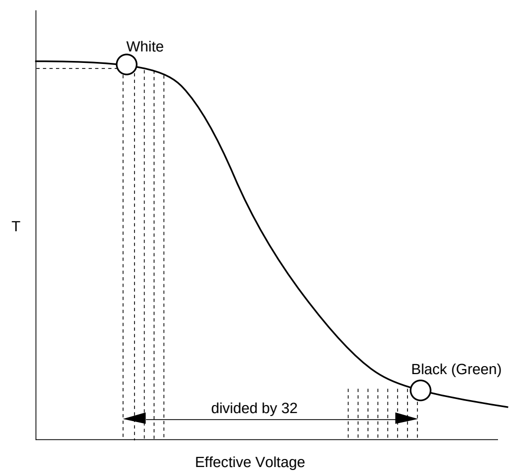


Figure 6 Effective Voltage Values vs. Transmittance

Grayscale Palette

The HD66522 is designed to generate 32 grayscale levels and provide palette registers that assign desired levels to certain of the 4 grayscale display. These grayscale palettes are addressed to H'1FF00 to H"1FF03 and initialized with RESET. The address and default value to grayscale palettes, and the relationships between grayscales and corresponding effective applied voltages are shown in Table 1.

Table 1 Grayscale Palette

Address	Data in memory	Register Name	Default value
H'1FF00	(1, 1)	GP11	(1, 1, 1, 1, 1)
H'1FF01	(0, 0)	GP00	(0, 0, 0, 0, 0)
H'1FF02	(0, 1)	GP01	(0, 1, 0, 1, 1)
H'1FF03	(1, 0)	GP10	(1, 0, 0, 1, 1)

Value					Effective voltage	Grayscale
4	3	2	1	0		
0	0	0	0	0	0	White
0	0	0	0	1	2/32	↓
0	0	0	1	0	3/32	
0	0	0	1	1	4/32	
0	0	1	0	0	5/32	
0	0	1	0	1	6/32	
0	0	1	1	0	7/32	
0	0	1	1	1	8/32	
0	1	0	0	0	9/32	
0	1	0	0	1	10/32	
0	1	0	1	0	11/32	
0	1	0	1	1	12/32	
0	1	1	0	0	13/32	
0	1	1	0	1	14/32	
0	1	1	1	0	15/32	
0	1	1	1	1	16/32	
1	0	0	0	0	17/32	
1	0	0	0	1	18/32	
1	0	0	1	0	19/32	
1	0	0	1	1	20/32	
1	0	1	0	0	21/32	
1	0	1	0	1	22/32	
1	0	1	1	0	23/32	
1	0	1	1	1	24/32	
1	1	0	0	0	25/32	
1	1	0	0	1	26/32	
1	1	0	1	0	27/32	
1	1	0	1	1	28/32	
1	1	1	0	0	29/32	
1	1	1	0	1	30/32	
1	1	1	1	0	31/32	
1	1	1	1	1	32/32	Black

Note : Based on the normally white LCD panel.

Address Management

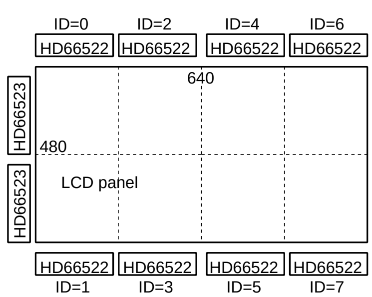
The HD66522 has an address management function that corresponds to four display sizes all of which are standard sizes for portable information devices: a 160-dot-wide by 240-dot-long display (small information devices); a 320-dot-wide by 240-dot-long display (quarter VGA size); a 320-dot-wide by 480-dot-long display (half VGA size); and a 640-dot-wide by 480-dot-long display (VGA size). Up to eight HD66522s can be connected to at a time to configure easily liquid crystal displays with the resolutions mentioned above.

Driver Layout and Address Management

The Y lines on a liquid crystal panel and memory data in a driver are inverted horizontally depending on the connection side of the liquid crystal panel and the driver. When several drivers are connected, address management is needed for each driver. Although reinverted bit-map plotting or address management by the $\overline{CS}$ pin in each driver are possible by using special write addressing, the load on the software is significantly increased. To avoid this, the HD66522 provides memory addresses independent of connection side, but responds to the setting of pins LS0, LS1, LS2 and SHL.

How to Use the LS2, LS1 and LS0 Pins

Pins LS2, LS1 and LS0 set the position (up to eight) as shown in Figure 7 by assigning ID numbers 0 to 7 to each HD66522.



LS2	LS1	LS0	ID No.	RAM Address Arrangement
L	L	L	0	Upper-side Left to Right
L	H	L	2	
H	L	L	4	
H	H	L	6	
L	L	H	1	Lower-side Left to Right
L	H	H	3	
H	L	H	5	
H	H	H	7	

L: Low Level H: High Level

Figure 7 LS0, LS1 and LS2 Pin Setting and Internal Memory Map

How to Use the SHL Pin

It is possible to invert the relationship between the addresses and output pins Y1 to Y160 by setting the SHL pin (Figure 8). The upper left section on the screen can be assigned to address H'00000 regardless of which side of the LCD panel the HD66522 is connected to.

The Relationship between the Data Bus and Output Pins

The 8-bit data on the data bus has a 2-bit/pixel configuration for a 4-level grayscale display. In addition, the 8-bit data on the data bus has a relationship as shown in table regardless of the relationship between pins LS0, LS1, LS2 and SHL. Since the relationship between data bus pins DB0 to DB7 and the output location are fixed, connect the data from the CPU directly to data bus pins DB0 to DB7.

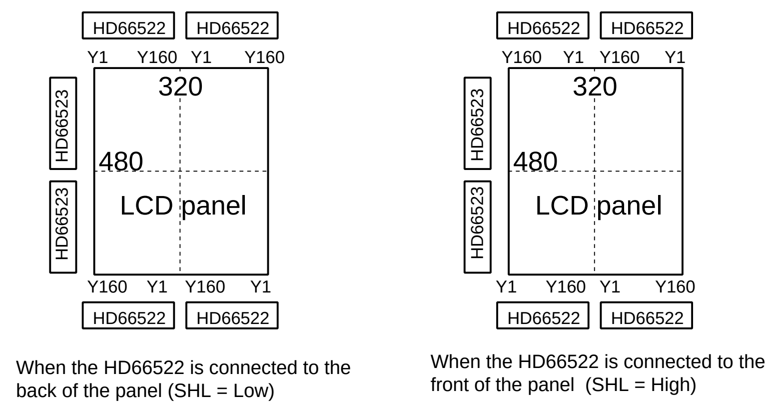


Figure 8 Address assignment and SHL Pin Setting

Table 2 Data Bus and Output Pins

Data Bus	Output Pins							
	SHL = Low				SHL = High			
DB0, DB1	Y1	Y5	....	Y157	Y160	....	Y8	Y4
DB2, DB3	Y2	Y6	....	Y158	Y159	....	Y7	Y3
DB4, DB5	Y3	Y7	....	Y159	Y158	....	Y6	Y2
DB6, DB7	Y4	Y8	....	Y160	Y157	....	Y5	Y1

Application Example

The HD66522 is suitable for a 160-dot-wide by 240-dot-long display (small information devices); a 320-dot-wide by 240-dot-long display (quarter VGA size); a 320-dot-wide by 480-dot-long display (half VGA size); and a 640-dot-wide by 480-dot-long display (VGA size). All of these are standard sizes for portable information devices. The following shows the system configuration.

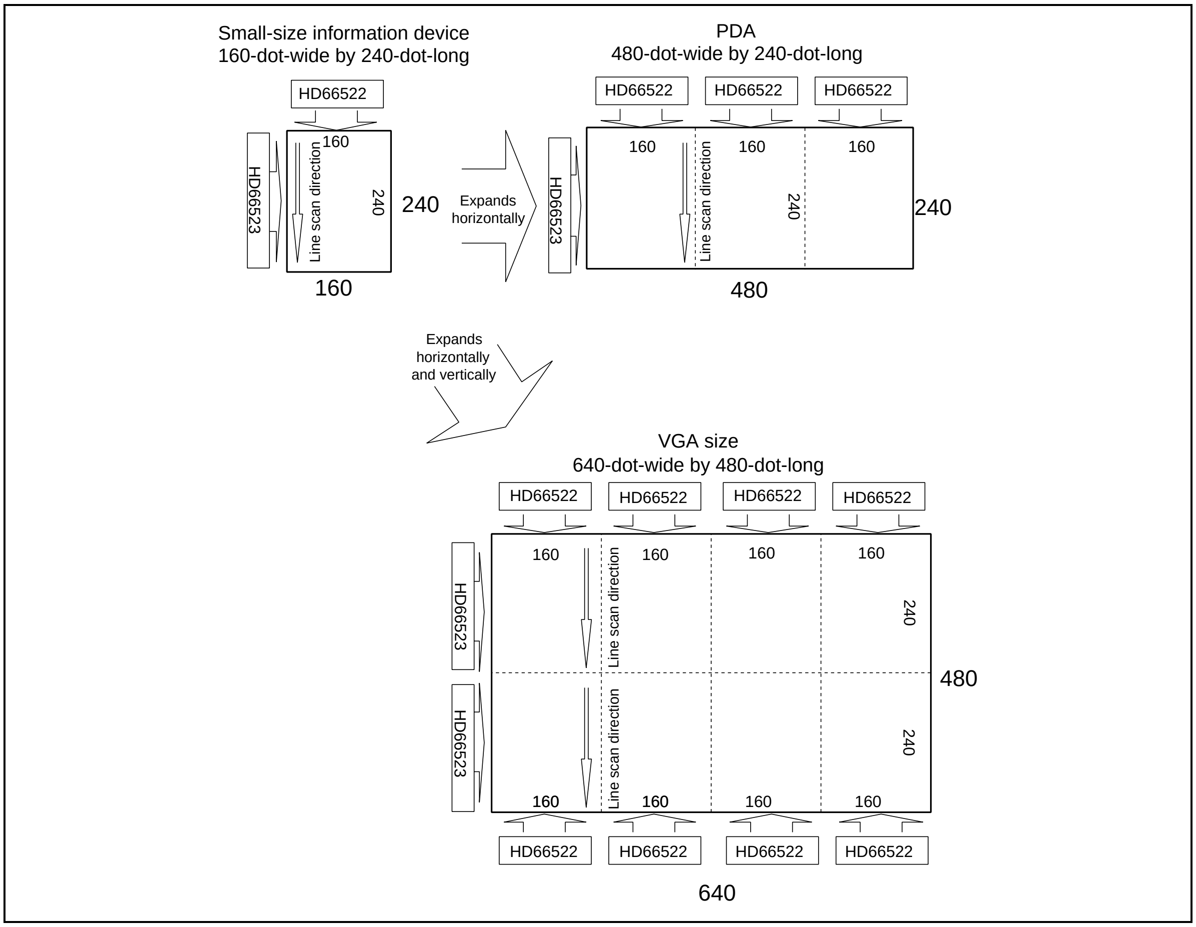


Figure 9 Application Examples

Small Information Device (SHL = Low)

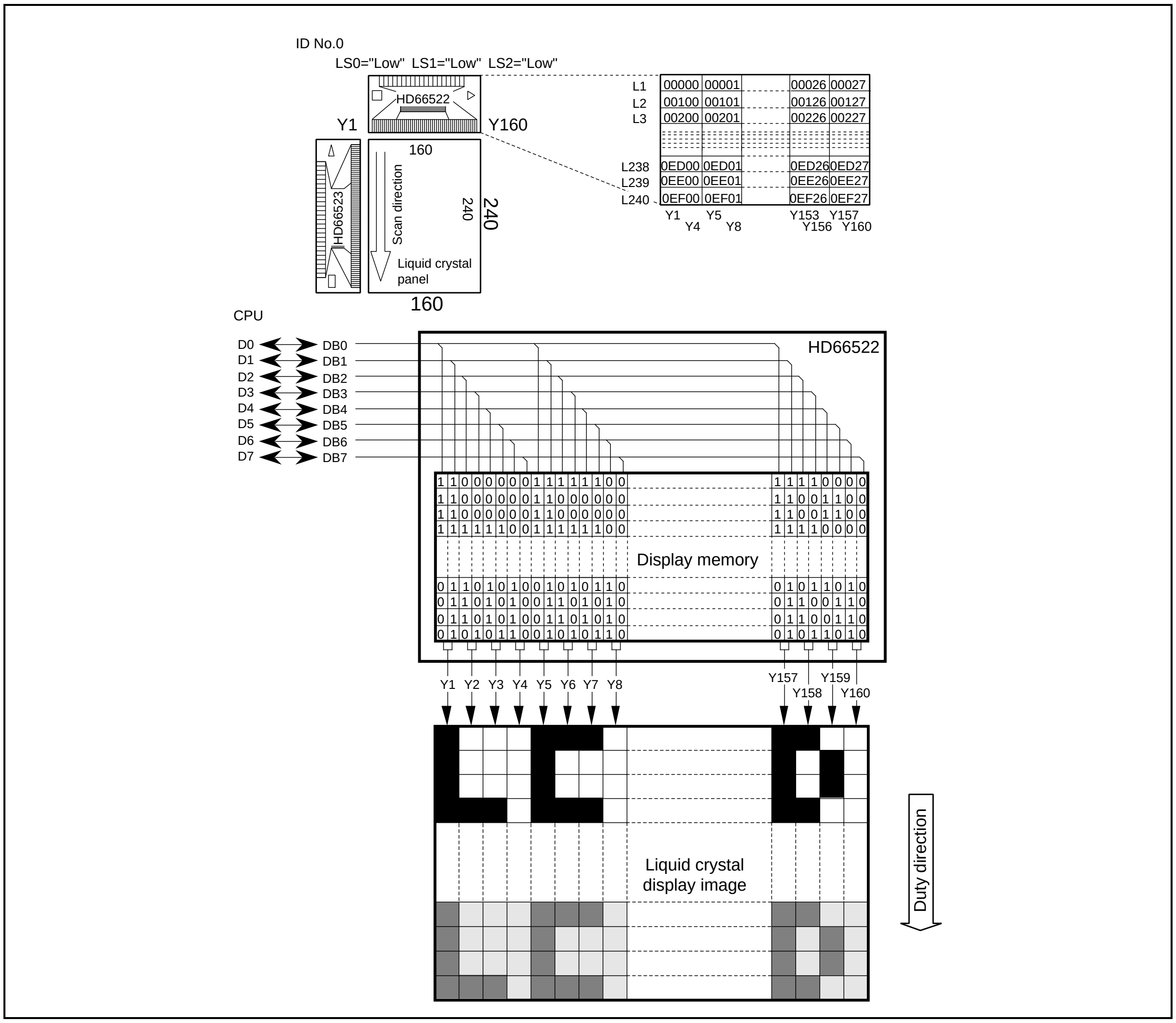


Figure 10 Small Information Device (1)

Small Information Device (SHL = High)

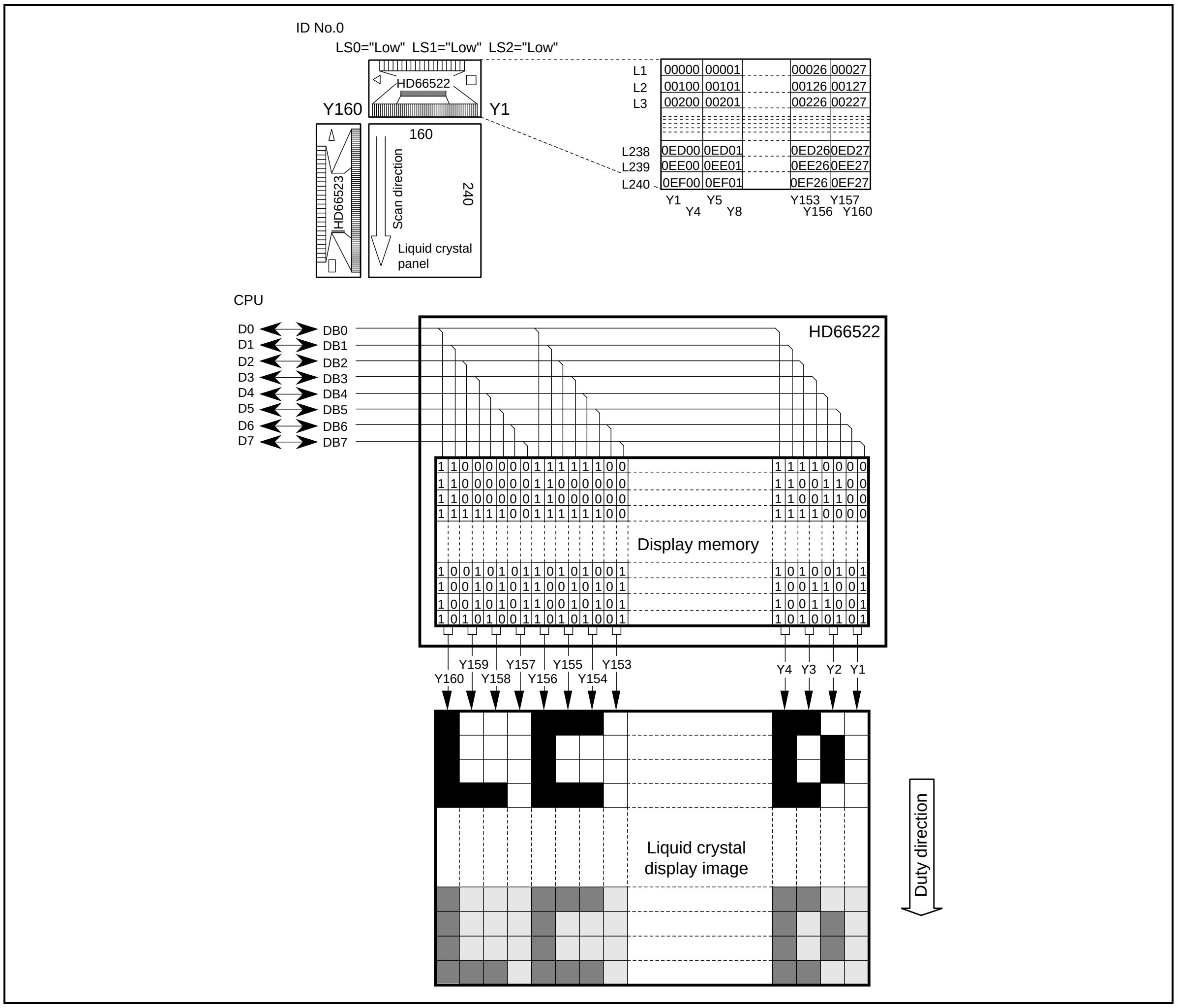


Figure 11 Small Information Device (2)

Quarter VGA Size (SHL = Low)

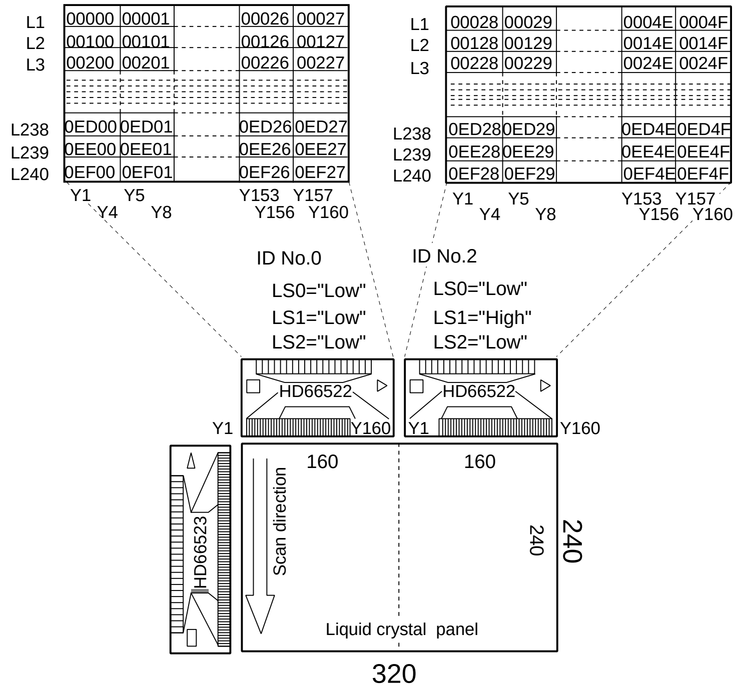


Figure 12 Quarter VGA Size (1)

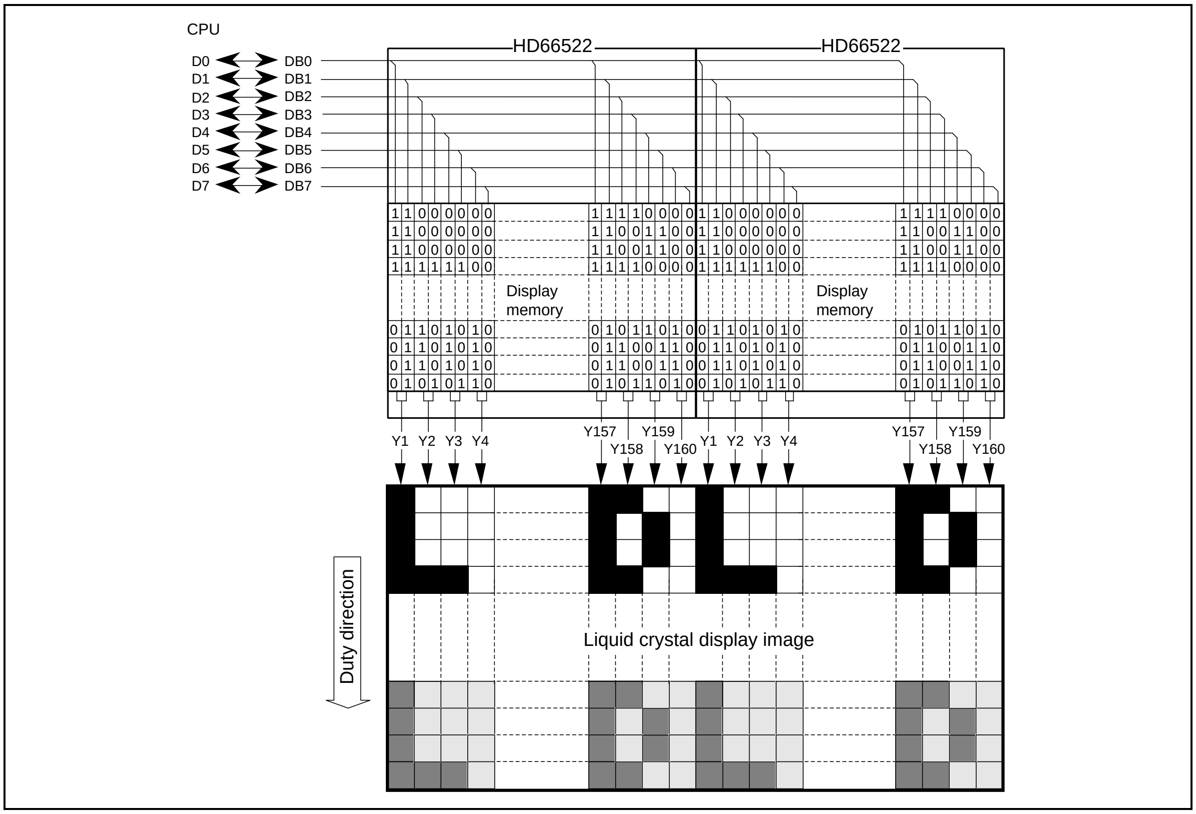


Figure 13 Quarter VGA Size (2)

Quarter VGA Size (SHL = High)

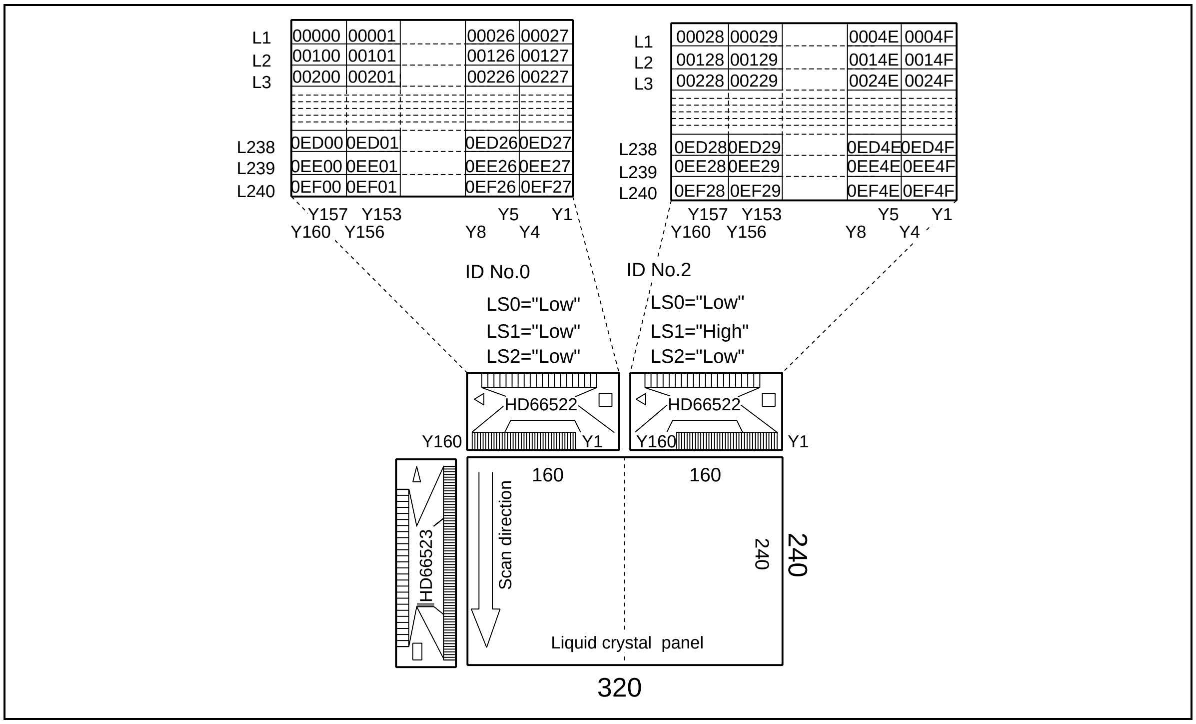


Figure 14 Quarter VGA Size (3)

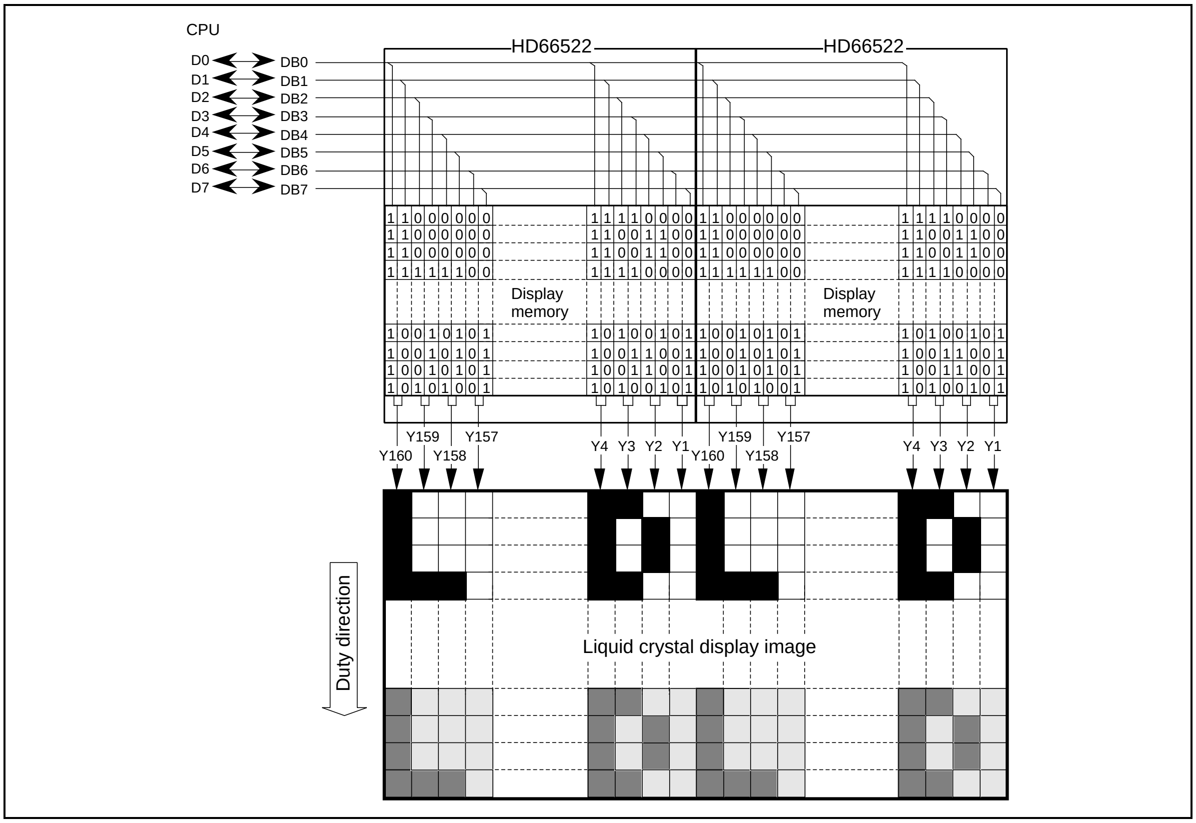


Figure 15 Quarter VGA Size (4)

Half VGA Size (SHL = Low)

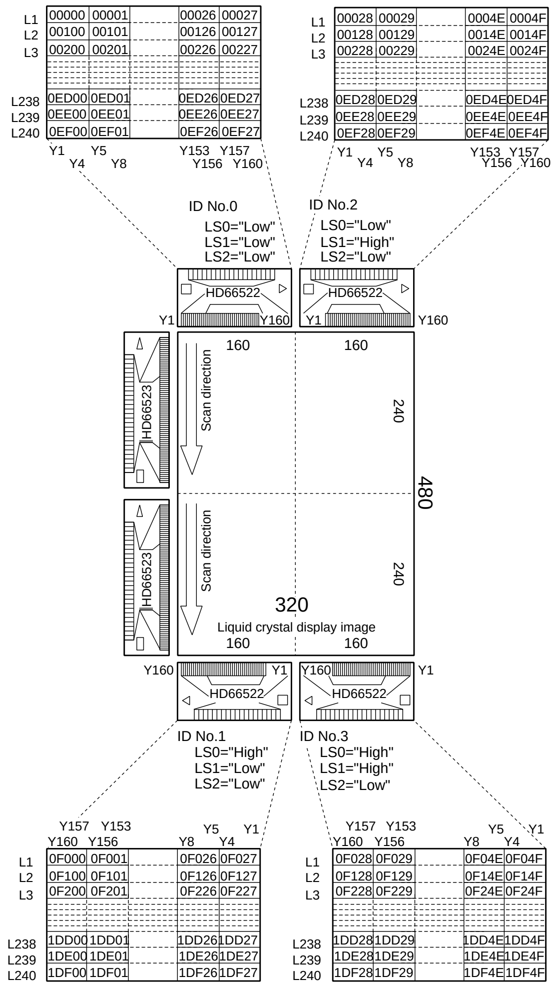


Figure 16 Half VGA Size (1)

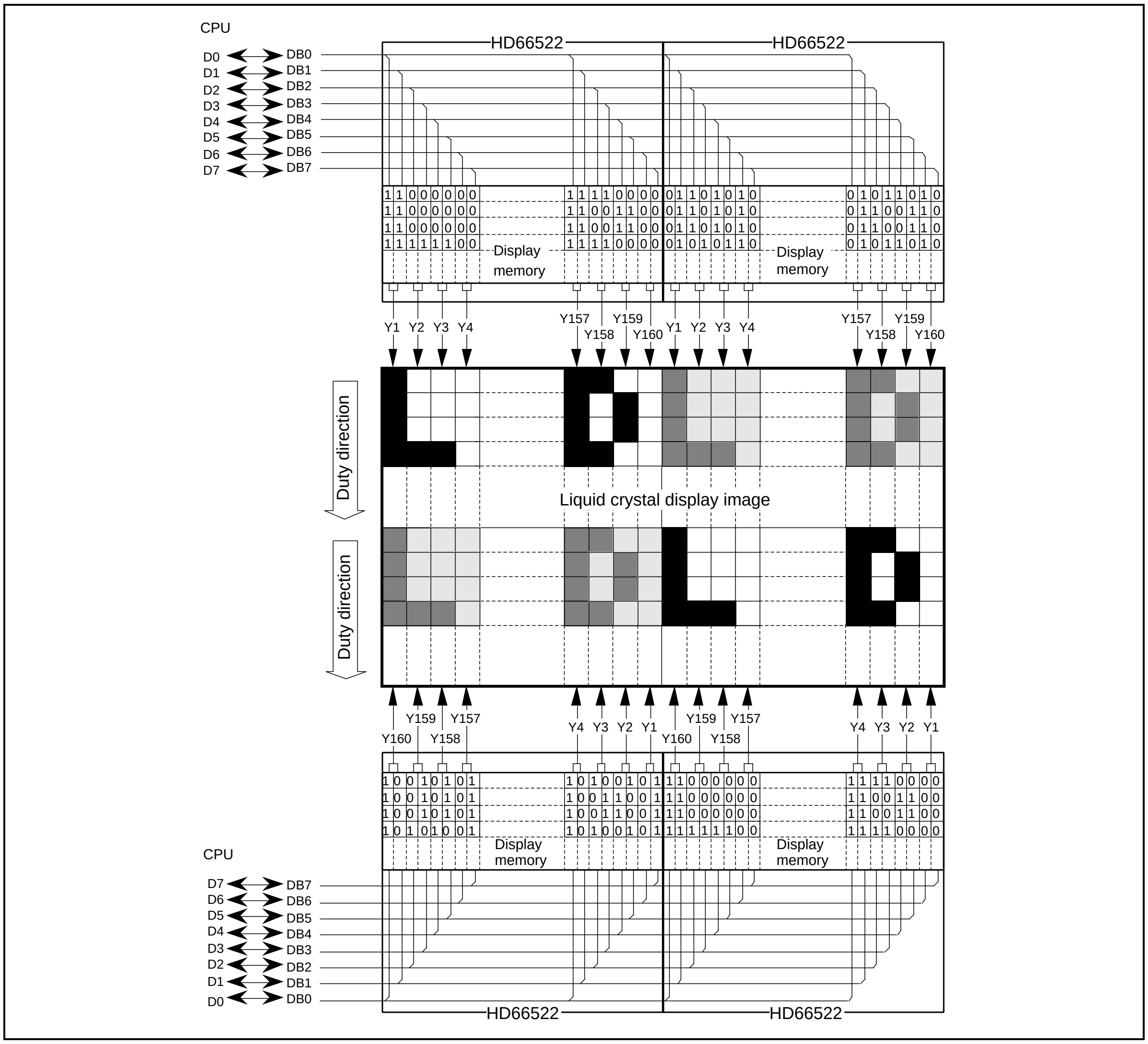


Figure 17 Half VGA Size (2)

Half VGA Size (SHL = High)

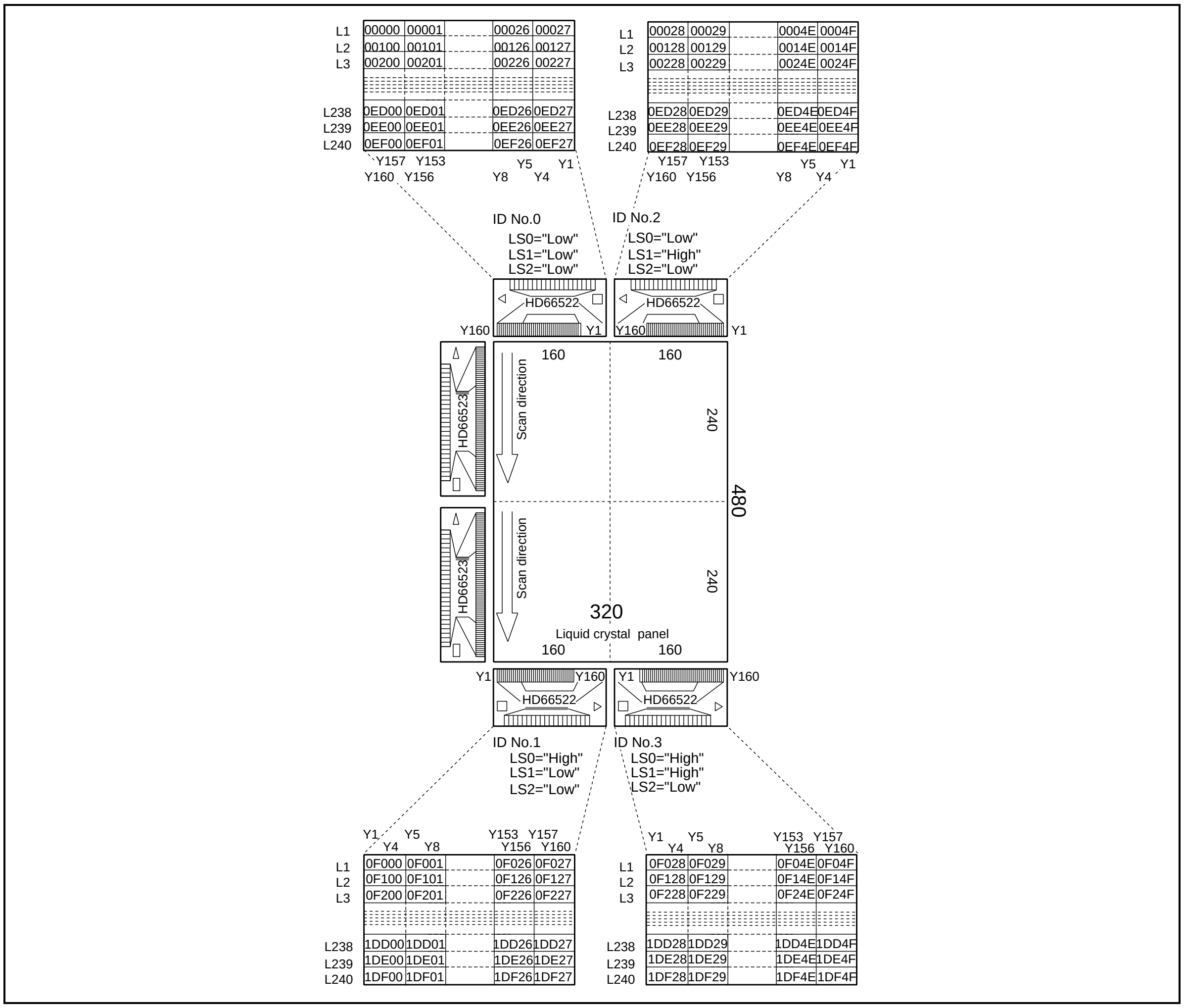


Figure 18 Half VGA Size (3)

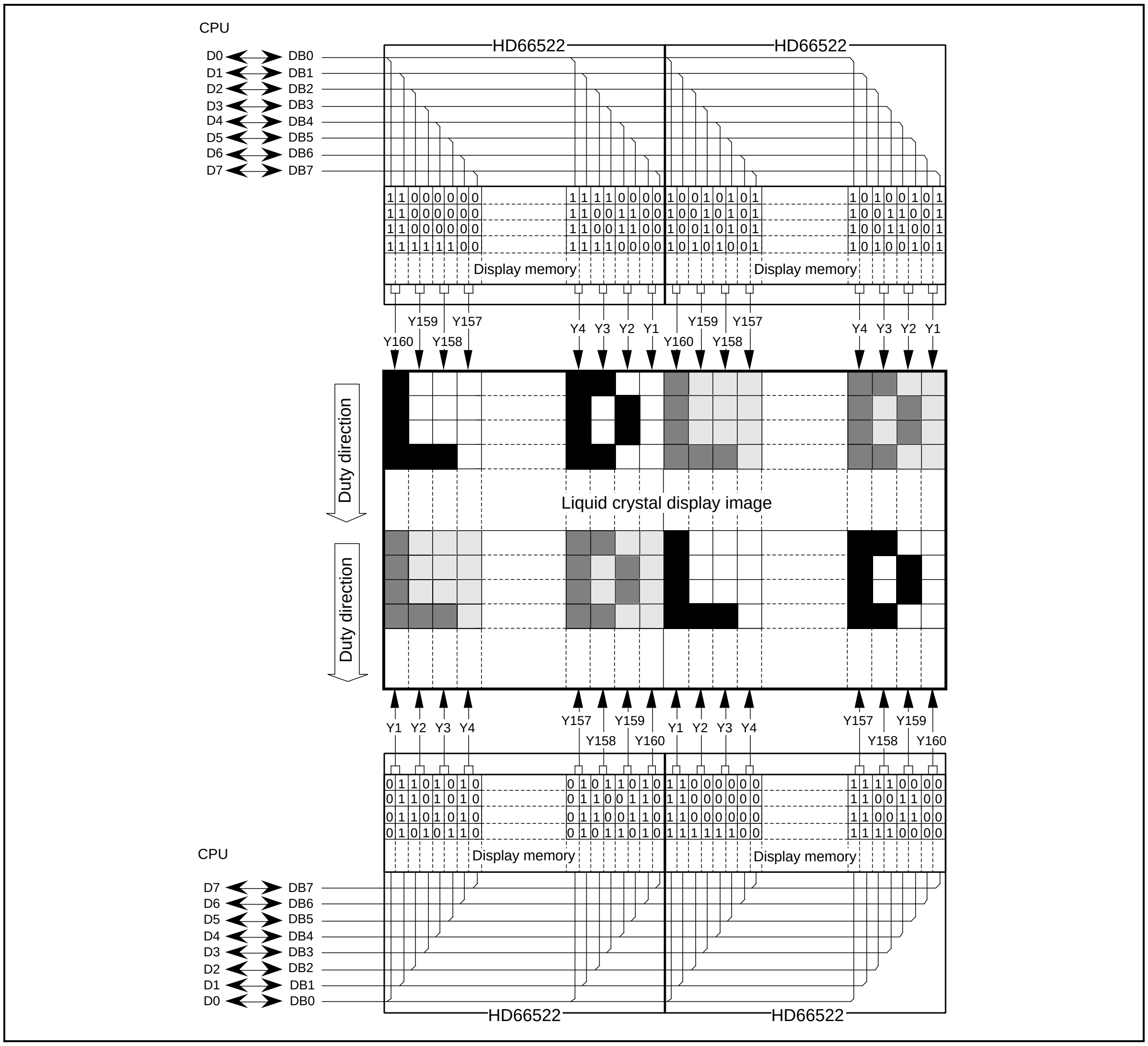


Figure 19 Half VGA Size (4)

VGA Size (SHL = Low)

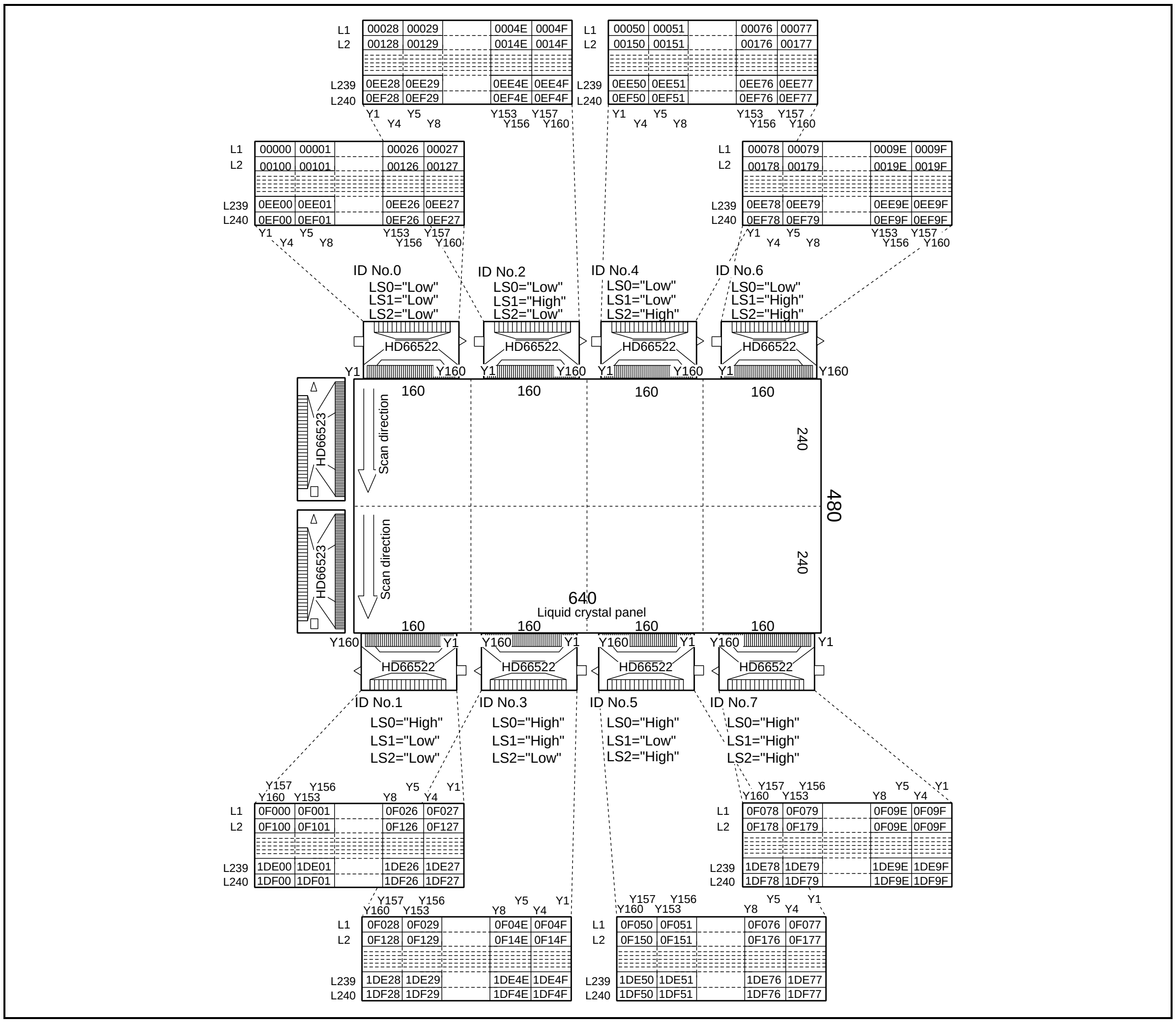


Figure 20 VGA Size (1)

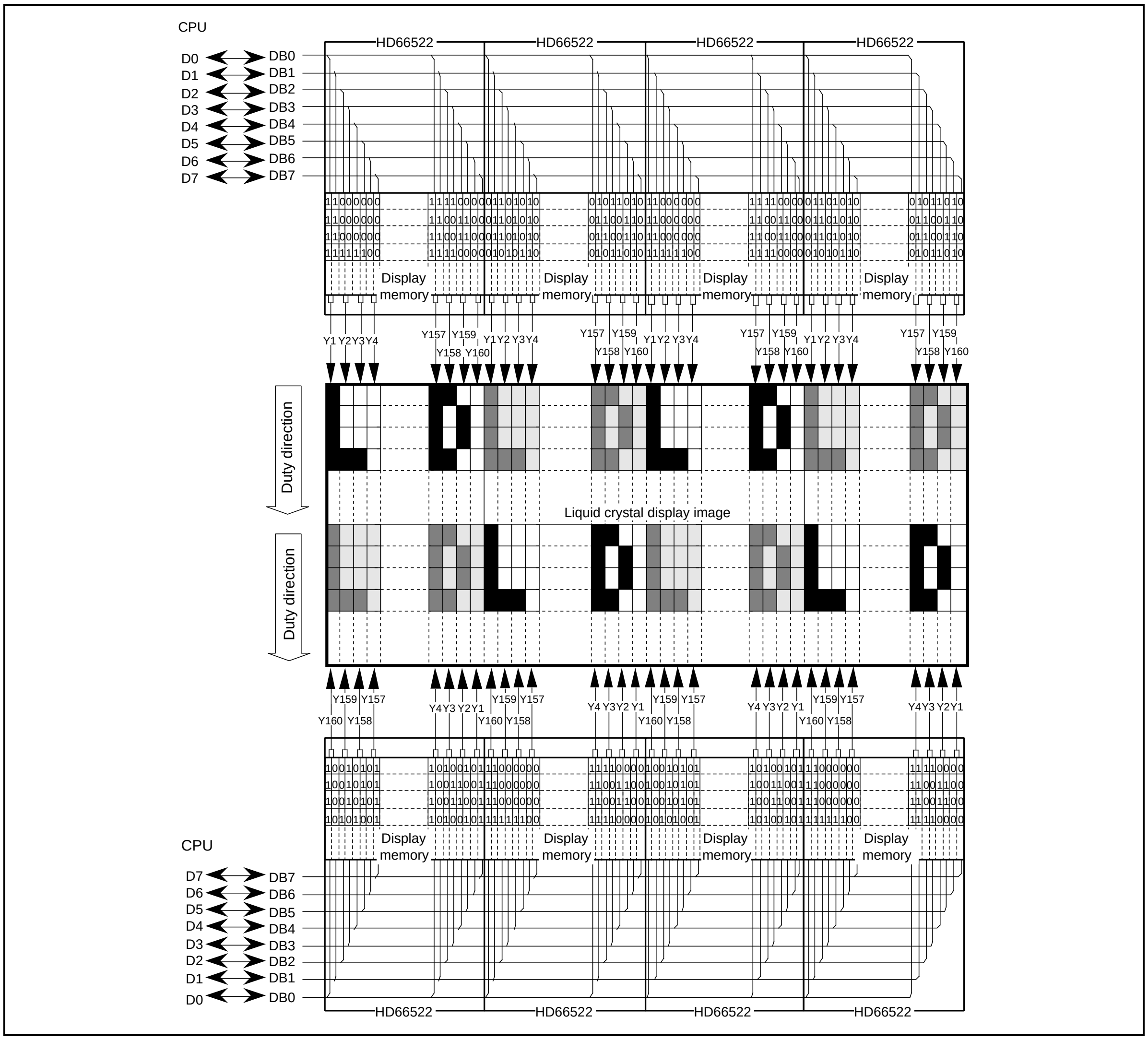


Figure 21 VGA Size (2)

VGA Size (SHL = High)

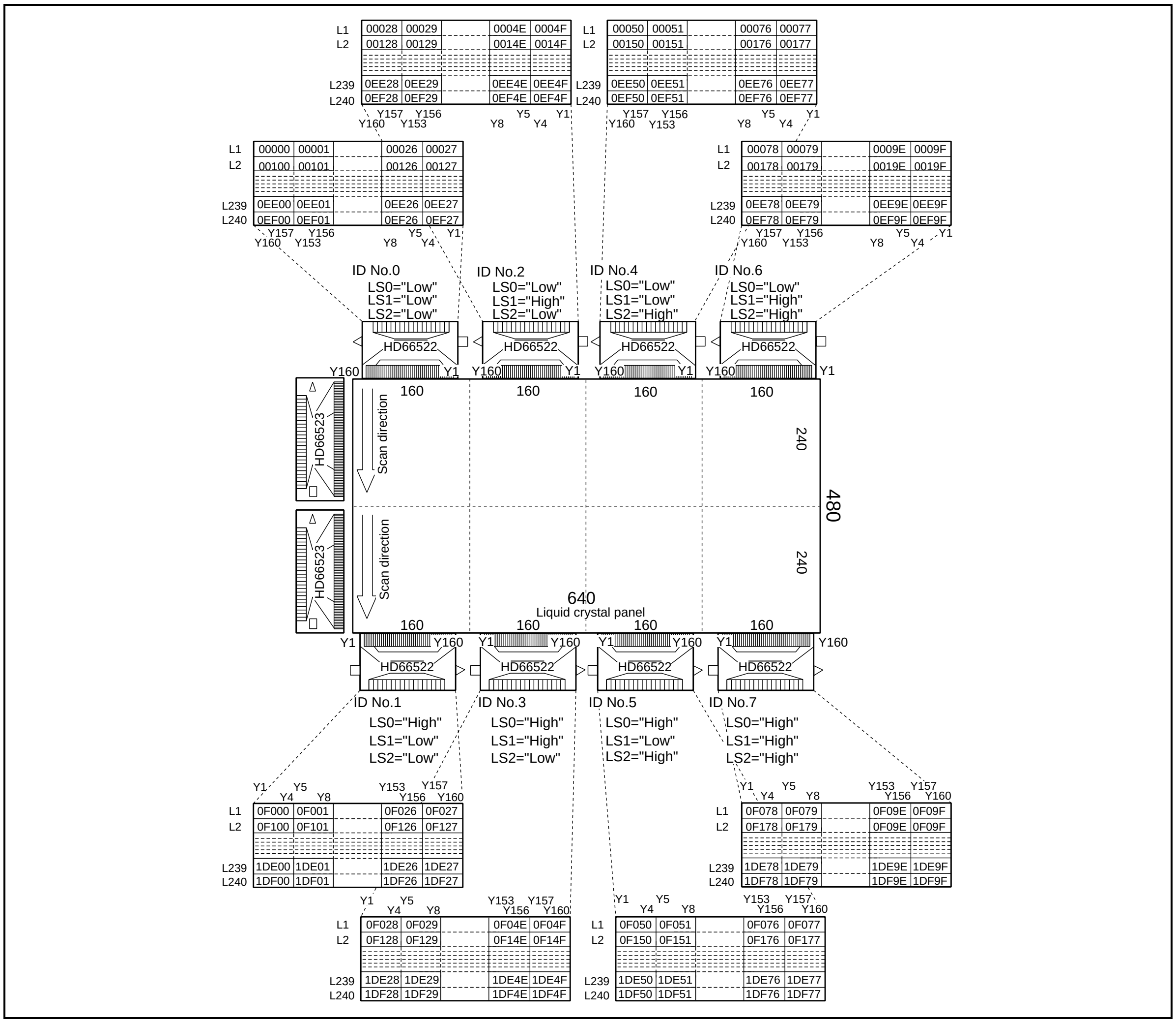


Figure 22 VGA Size (3)

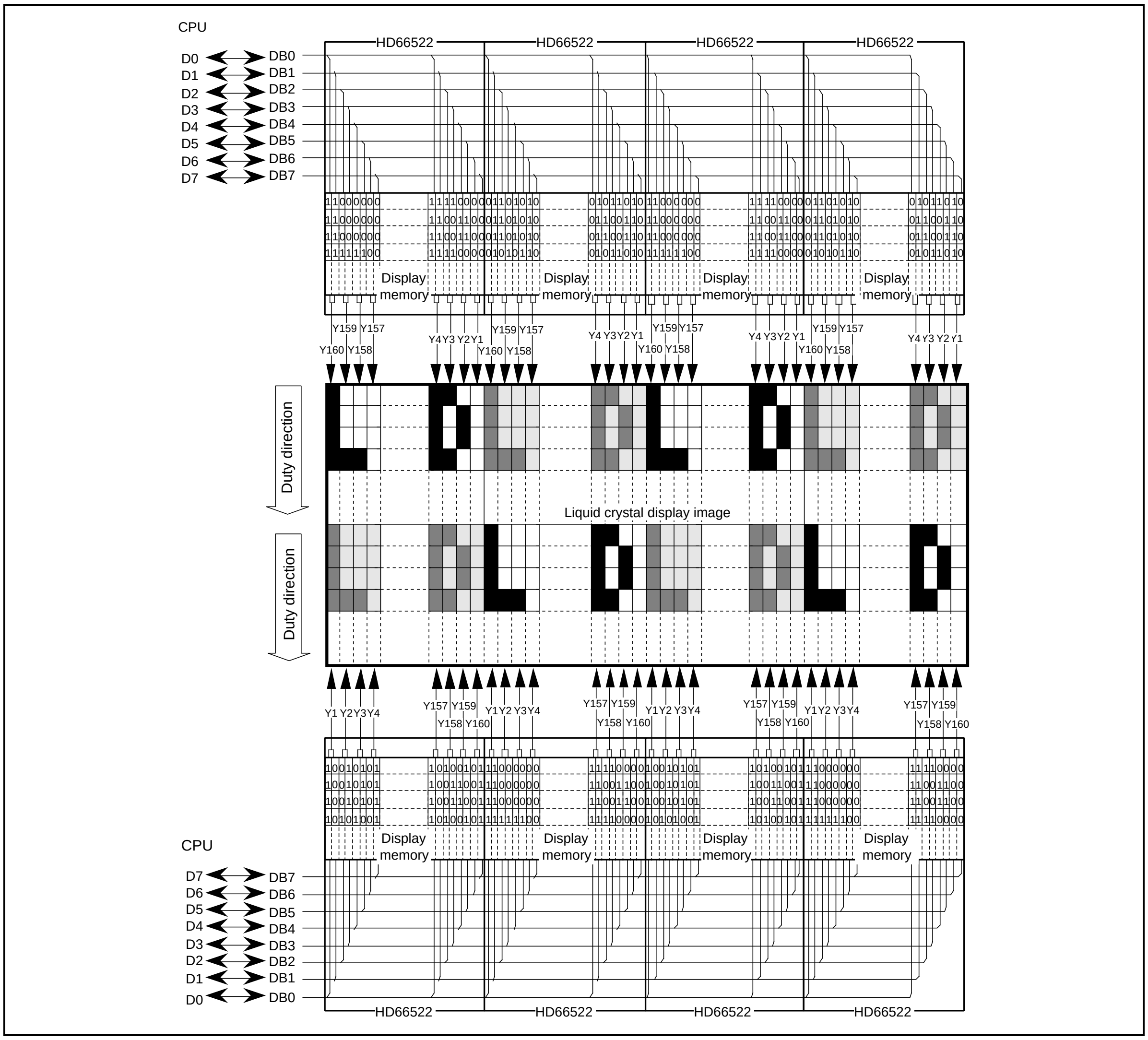


Figure 23 VGA Size (4)

Display Data Transfer

Display RAM data is transferred to 160-bit data latch circuit 1 at each falling edge of the CL1 clock pulse. Since display data transfer and RAM access to draw data are completely asynchronous in the LSI, there will be no draw data loss or display flickering due to display data transfertiming.

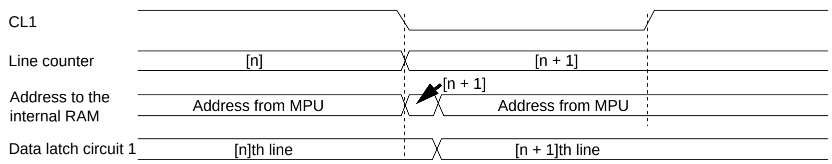


Figure 24 Display Data Transfer

Draw Access

Random cycle

Random cycle sequence is the same as that for the general-purpose SRAM interface (Figures 25 and 26). It can easily be connected to a CPU address bus and data bus.

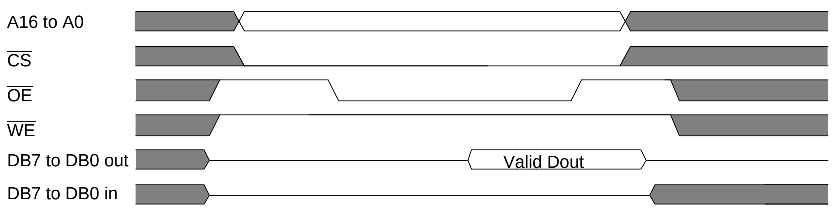


Figure 25 Read Cycle

Figure 26 Write Cycle

Burst Cycle

Continuous access (burst cycle) can be performed by enabling addresses and $\overline{OE}$ or $\overline{WE}$ when $\overline{CS}$ is low (Figures 27 and 28).

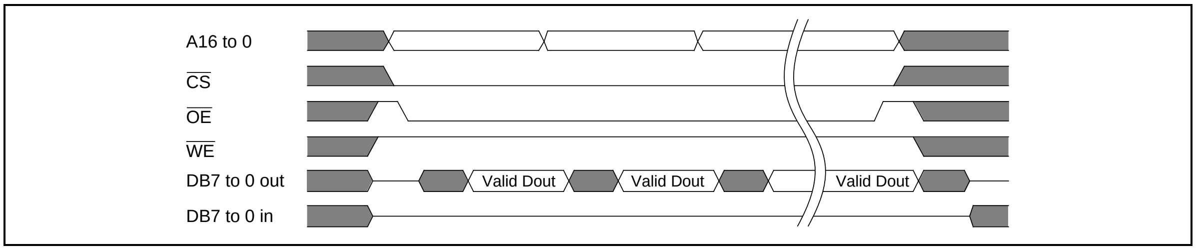


Figure 27 Burst Read Cycle

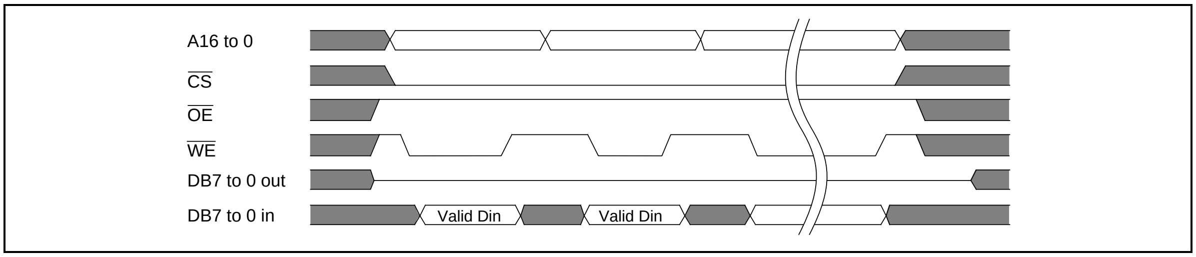


Figure 28 Burst Write Cycle

Arbitration Control

HD66522 controls the arbitration between draw access and display access. The draw access reads and writes display data of the display memory incorporated in the HD66522. The display access outputs display memory line data to the liquid crystal panel. If these accesses occur at the same time, HD66522 outputs $\overline{\text{WAIT}}$ signal and halt draw access. The bus cycle must be extended until display access finishes with using this $\overline{\text{WAIT}}$ signal.

Display Access without Draw Access: If no draw access is attempted, normal display access is performed after the falling edge of CL1. (Figure 29)

Collision between Display Access and Draw Access (1): When the draw access occurs during the display access, $\overline{\text{WAIT}}$ goes low at the falling edge of $\overline{\text{WE}}$ or $\overline{\text{OE}}$ and goes high at the end of the display access. The draw access must be extended with using this $\overline{\text{WAIT}}$ signal.

Collision between Display Access and Draw Access (2): When the display access occurs during the draw access, the display access halts until the draw access finishes. $\overline{\text{WAIT}}$ goes low at the end of the draw access, transition point of address or the rising edge of $\overline{\text{WE}}$ of $\overline{\text{OE}}$, and goes high at the end of display access. The draw access must be extended with using this $\overline{\text{WAIT}}$ signal.

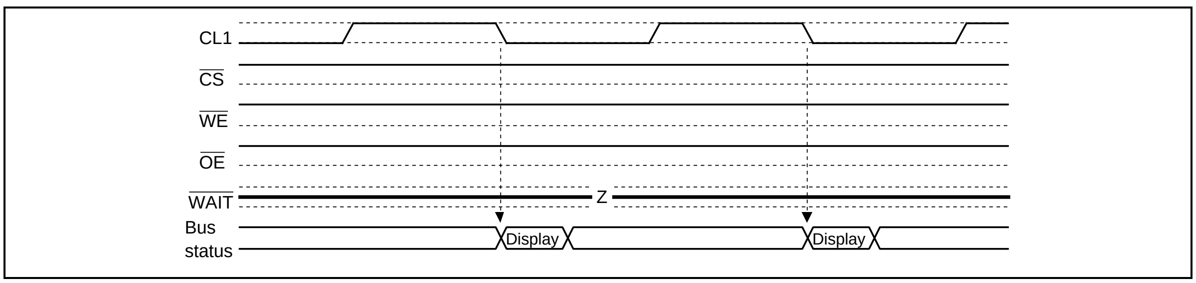


Figure 29 Display Access

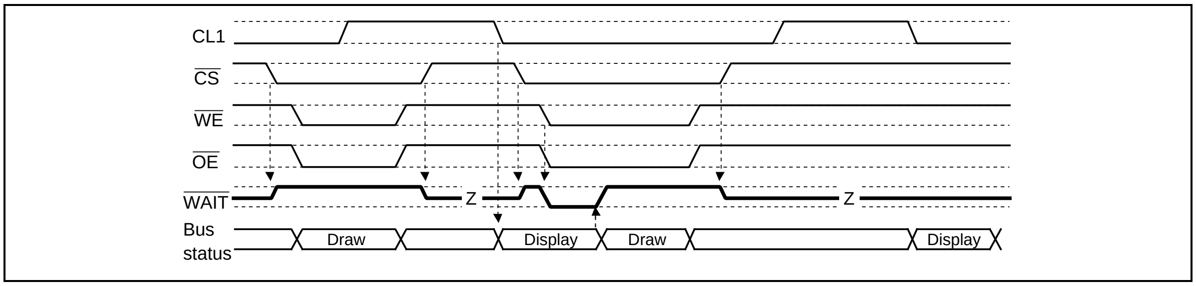


Figure 30 Collision Between Display Access and Draw Access (1)

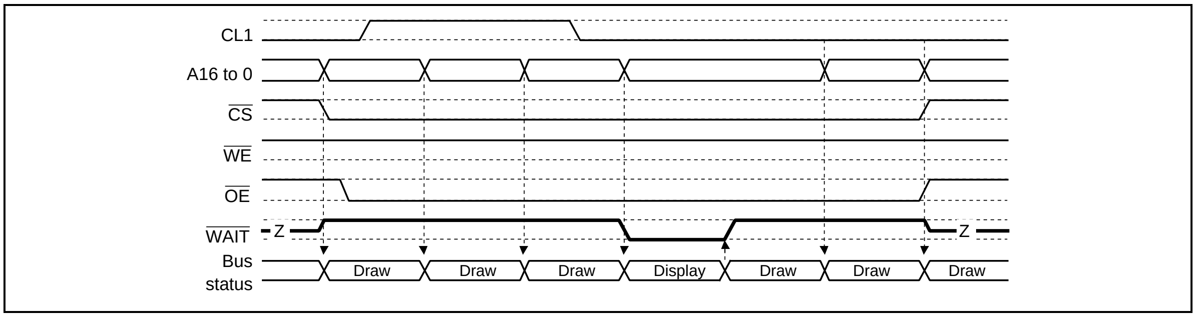


Figure 31 Collision Between Display Access and Draw Access (2)

Example of System Configuration

Figure 32 shows a system configuration for a 320-bit-wide by 240-dot-long LCD panel using two HD66522s and common driver HD66523 with internal liquid crystal display timing control circuits. All required functions can be prepared for liquid crystal display with just three chips except for liquid crystal display power supply circuit functions.

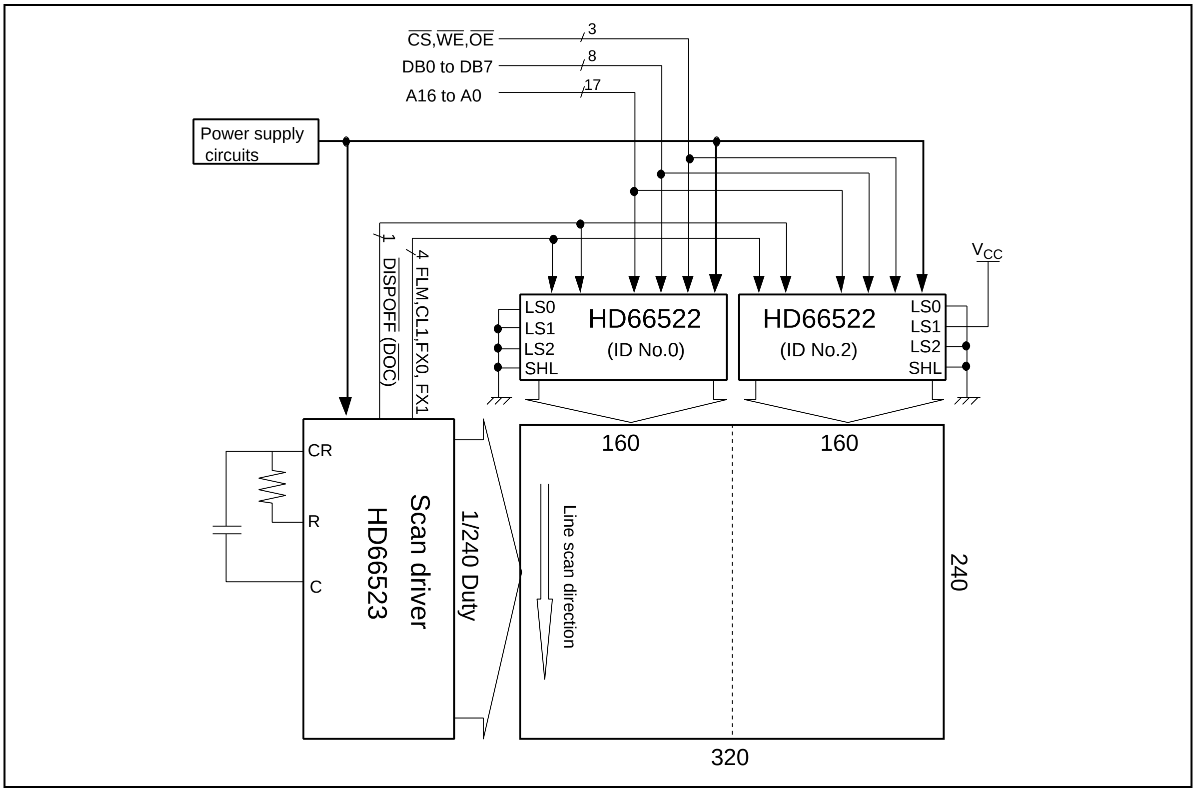


Figure 32 System Configuration

Power Supply circuit

To drive the LCD using multi-line technique, 5-level power supply is necessary; two for HD66522, two for HD66523 and one for both. These levels can be generated by dividing the VRH–VRL power supply using resistive divider and buffered with voltage followers to reduce impedance. Figure 33 shows a example of the power supply circuit. A DC/DC convertor module which generates all voltages is used in this circuit. The voltages which are supplied to VCL, VCH and VM must keep following equations:

GND < VCL
VM = 1/2 (VRH–VRL) = 1/2 (VCH–VCL)
4V < VCH < 6V

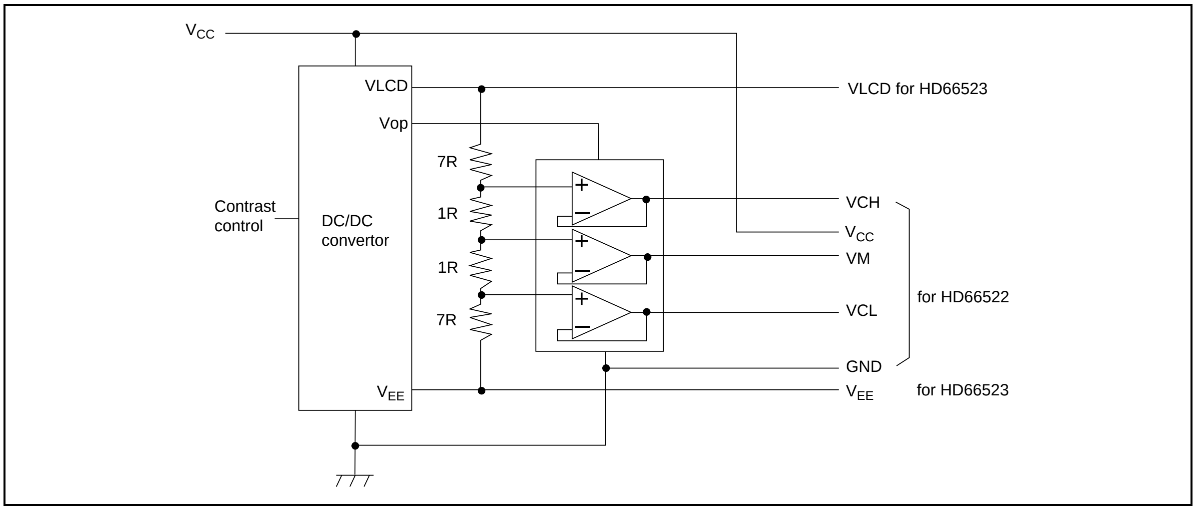


Figure 33 Example of power supply circuit

Absolute Maximum Ratings

Item	Symbol	Rating	Unit	Note	
Power voltage	Logic circuit	V_{CC}	–0.3 to +7.0	V	1
	LCD drive circuit	VCH	–0.3 to +7.0	V	
Input voltage (1)		V_{T1}	–0.3 to V_{CC} +0.3	V	1, 2
Input voltage (2)		V_{T2}	–0.3 to VCH +0.3	V	1, 3
Operating temperature		Topr	–20 to +75	°C	
Storage temperature		Tstg	–40 to +125	°C	

Notes:
1. The reference point is GND (0V).
2. Applies to pins LS0 to LS2, SHL, FLM, CL1, FX0, FX1, A0 to A16, DB0 to DB7, $\overline{DISPOFF}$, $\overline{CS}$, $\overline{WE}$, $\overline{OE}$ and $\overline{WAIT}$.
3. Applies to pins VM1, VM2, VCL1 and VCL2.
4. If the LSI is used beyond its absolute maximum rating, it may be permanently damaged. It should always be used within the limits of its electrical characteristics in order to prevent malfunction or unreliability.

Electrical Characteristics

DC Characteristics 1 (V_{CC} = 2.4 to 3.6V, GND = 0V, VCH = 4 to 6V, Ta = –20 to +75 °C)

Item	Symbol	Applicable Pins	min.	typ.	max.	Unit	Measurement Condition	Notes
Input high level voltage	V_{IH1}	LS0-2,SHL,FLM, CL1,M, $\overline{DISPOFF}$	$0.8 \times V_{CC}$	—	V_{CC}	V		
Input low level voltage	V_{IL1}		0	—	$0.2 \times V_{CC}$	V		
Output high level voltage	V_{OH}	DB0 to DB7	$0.9 \times V_{CC}$	—	—	V	I_{OH} = –50 µA	
Output low level voltage	V_{OL}		—	—	$0.1 \times V_{CC}$	V	I_{OL} = 50 µA	
Input leakage current (1)	I_{IL1}	except DB0 to DB7	–2.5	—	2.5	µA	VIN = V_{CC} to GND	
Input leakage current (2)	I_{IL2}	VCL1,VCL2, VM1,VM2	–25	—	25	µA	VIN = VCH to GND	
Tri-state leakage current	I_{IST}	DB0 to DB7	–10	—	10	µA	VIN = V_{CC} to GND	
Vi-Yj ON resistance	R_{ON}	Y1 to Y160	—	1.0	2.0	KΩ	I_{ON} = 100 µA	1
Current consumption during RAM access	I_{CC}	V_{CC}	—	—	T.B.D.	mA	access cycle time: 120 ns V_{CC} = 3.3V	2
Current consumption in LCD drive part	I_{EE}	V_{EE}	—	—	T.B.D.	µA	V_{CC} = 3.3V VCH = 6V t_{CYC} = 59.5 µs no access form MPU	2
Current consumption during display operation	I_{DIS}	GND	—	—	T.B.D.	µA		3

Notes: 1. Indicates the resistance between one pin from Y1 to Y160 and another pin from VCH1/2, VCL1/2, VM1/2

when load current is applied to the Y pin; defined under the following condition:

VCH = 6.0V

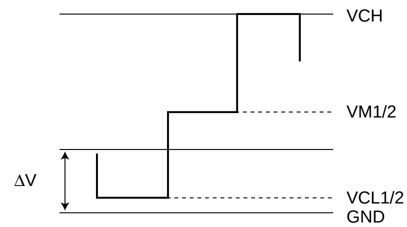
VM = 1/2 (VCH–VCL)

VCL = 1.0V

VM1/2 should be near the center between VCH level and VCL level, and VCL should be near the GND level. VCL must be within ÆV = 0.3 × VCH. ÆV is the range within which R_{ON}, the LCD driver circuit output impedance, is stable.

2. Input and output currents are excluded. When a CMOS input is floating, excess current flows from the power supply through to the input circuit. To avoid this, VIH and VIL must be held to V_{CC} and GND levels, respectively.

3. Indicates the current when the display-operation memory access is stopped and the still image of a checker-board pattern in displayed in its place.



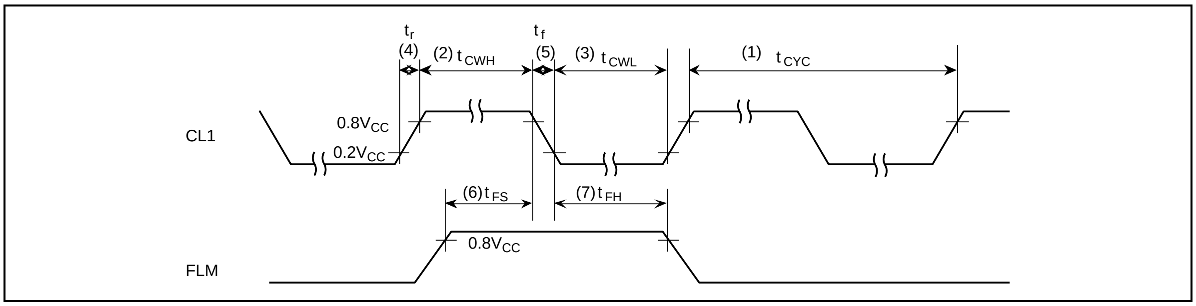
Relationship between Driver Output Waveform and Level Voltages

AC Characteristic 1 (V_{CC} = 2.4 to 3.6V, GND = 0V, VCH = 4 to 6V, Ta = –20 to +75°C)

- **Display-Data Transfer Timing**

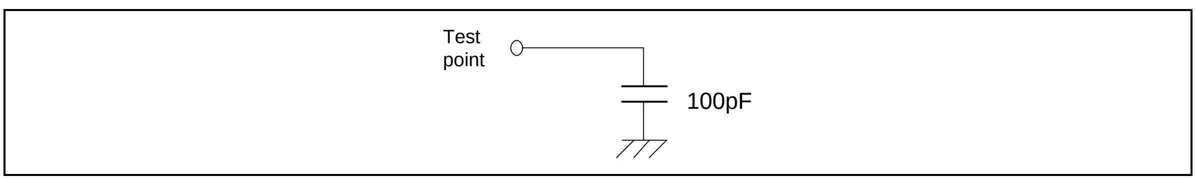
No.	Item	Symbol	Applicable Pins	min.	max.	Units	Notes
(1)	Clock cycle time	t_{CYC}	CL1	10	—	µs	1
(2)	CL1 high-level width	t_{CWH}	CL1	1.0	—	µs	
(3)	CL1 low-level width	t_{CWL}	CL1	1.0	—	µs	
(4)	CL1 rise time	t_r	CL1	—	50	ns	
(5)	CL1 fall time	t_f	CL1	—	50	ns	
(6)	FLM setup time	t_{FS}	FLM, CL1	2.0	—	µs	
(7)	FLM hold time	t_{FH}	FLM, CL1	1.0	—	µs	

Note: 1 $f_{CYC} = 1/t_{CYC}$
Max: 100KHz



Measurement Condition

Input level: $V_{IH} = 0.8 * V_{CC}$, $V_{IL} = 0.2 * V_{CC}$
Output Level: VOH = 1.5V, VOL = 1.5V
Output Load: 100pF



AC Characteristics 2 (V_{CC} = 2.7 to 3.6V, GND = 0V, VCH = 4 to 6V, Ta = –20 to +75 °C)

- **Access Timing**

— Read Cycle

No.	Item	Symbol	min.	max.	Units	Notes
(8)	Read cycle time	t_{RC}	120	—	ns	
(9)	Address access time	t_{AA}	—	120	ns	
(10)	Chip select access time	t_{CA}	—	120	ns	
(11)	Access-time from output-enable to output	t_{OE}	—	60	ns	
(12)	Set-time from output-enable to outpu	t_{OLZ}	5	—	ns	
(13)	Floating-time from output-disable to output	t_{OHZ}	0	40	ns	
(14)	Output hold time	t_{OH}	10	—	ns	

— Write Cycle

No.	Item	Symbol	min.	max.	Units	Notes
(15)	Write cycle time	t_{WC}	120	—	ns	
(16)	Chip select time	t_{CW}	85	—	ns	
(17)	Address setup time	t_{AS}	0	—	ns	
(18)	Address hold time	t_{WR}	0	—	ns	
(19)	$\overline{WE}$ low-level width	t_{WP}	70	—	ns	
(20)	Input data set time	t_{DW}	50	—	ns	
(21)	Input data hold time	t_{DH}	0	—	ns	

- **$\overline{WAIT}$ Output Timing**

No.	Item	Symbol	min.	max.	Units	Notes
(22)	$\overline{WAIT}$ delay time (low impedance)	t_{WLZ}	10	—	ns	
(23)	$\overline{WAIT}$ delay time (Read)	t_{RWE}	50	—	ns	
(24)	$\overline{WAIT}$ low level width (Read)	t_{RWW}	—	240	ns	
(25)	$\overline{WAIT}$ output-disable time	t_{WHZ}	—	30	ns	
(26)	$\overline{WAIT}$ access time	t_{OWE}	60	—	ns	
(27)	$\overline{WAIT}$ delay time (Write)	t_{WWE}	50	—	ns	
(28)	$\overline{WAIT}$ low level width (Write)	t_{WWW}	—	150	ns	

AC Characteristics 3 (V_{CC} = 2.4 to 2.7V, GND = 0V, VCH = 4 to 6V, Ta = –20 to +75 °C)

- **Access Timing**

— Read Cycle

No.	Item	Symbol	min.	max.	Units	Notes
(8)	Read cycle time	t_{RC}	160	—	ns	
(9)	Address access time	t_{AA}	—	160	ns	
(10)	Chip select access time	t_{CA}	—	160	ns	
(11)	Access-time from output-enable to output	t_{OE}	—	80	ns	
(12)	Set-time from output-enable to output	t_{OLZ}	5	—	ns	
(13)	Floating-time from output-disable to output	t_{OHZ}	0	50	ns	
(14)	Output hold time	t_{OH}	10	—	ns	

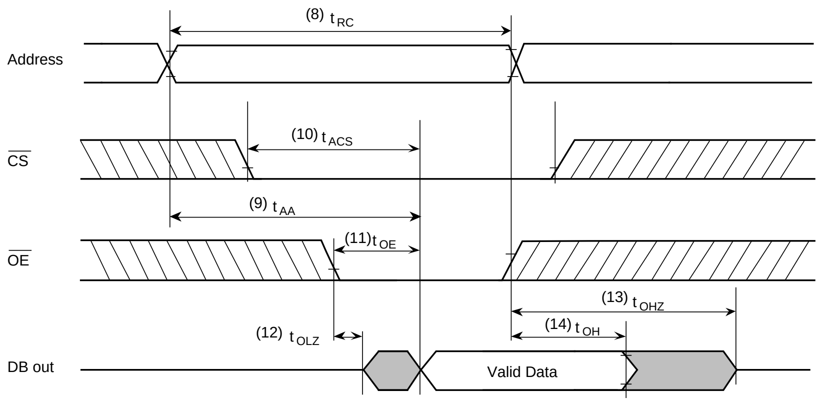
— Write Cycle

No.	Item	Symbol	min.	max.	Units	Notes
(15)	Write cycle time	t_{WC}	160	—	ns	
(16)	Chip select time	t_{CW}	100	—	ns	
(17)	Address setup time	t_{AS}	0	—	ns	
(18)	Address hold time	t_{WR}	0	—	ns	
(19)	$\overline{WE}$ low-level width	t_{WP}	100	—	ns	
(20)	Input data set time	t_{DW}	70	—	ns	
(21)	Input data hold time	t_{DH}	0	—	ns	

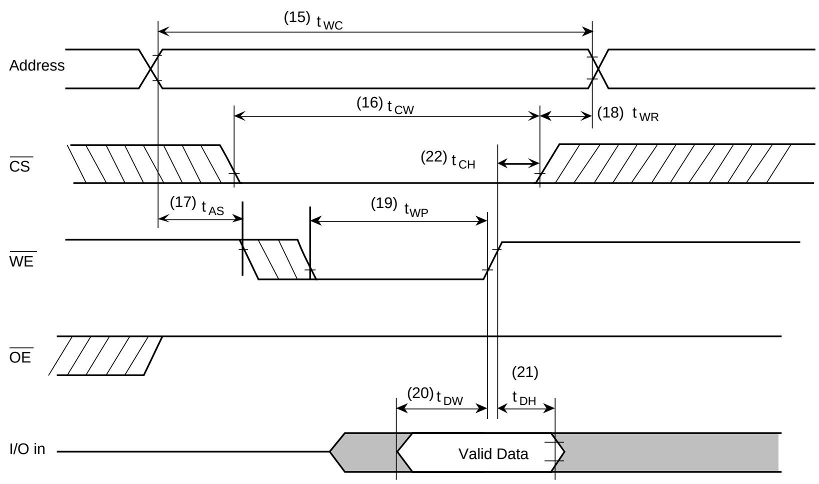
- **$\overline{WAIT}$ Output Timing**

No.	Item	Symbol	min.	max.	Units	Notes
(22)	$\overline{WAIT}$ delay time (low impedance)	t_{WLZ}	10	—	ns	
(23)	$\overline{WAIT}$ delay time (Read)	t_{RWE}	70	—	ns	
(24)	$\overline{WAIT}$ low level width (Read)	t_{RWW}	—	300	ns	
(25)	$\overline{WAIT}$ output-disable time	t_{WHZ}	—	40	ns	
(26)	$\overline{WAIT}$ access time	t_{OWE}	100	—	ns	
(27)	$\overline{WAIT}$ delay time (Write)	t_{WWE}	70	—	ns	
(28)	$\overline{WAIT}$ low level width (Write)	t_{WWW}	—	200	ns	

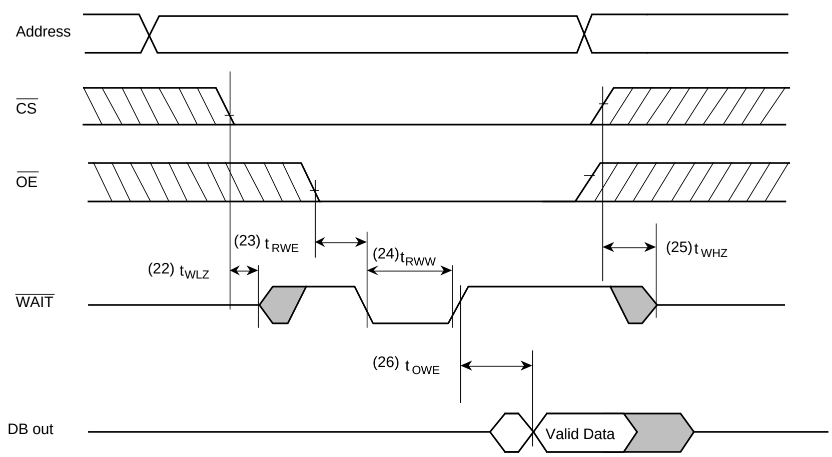
Read Cycle



Write Cycle



$\overline{\text{WAIT}}$ Output Timing (Read Cycle)



$\overline{\text{WAIT}}$ Output Timing (Write Cycle)