

LCD Product Line Selection Table

	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626	HT1627	HT16270
COM	4	4	8	8	8	8	16	16	16
SEG	32	32	32	32	48	64	48	64	64
Built-in Osc.		√	√		√	√	√	√	
Crystal Osc.	√	√		√					√

Features

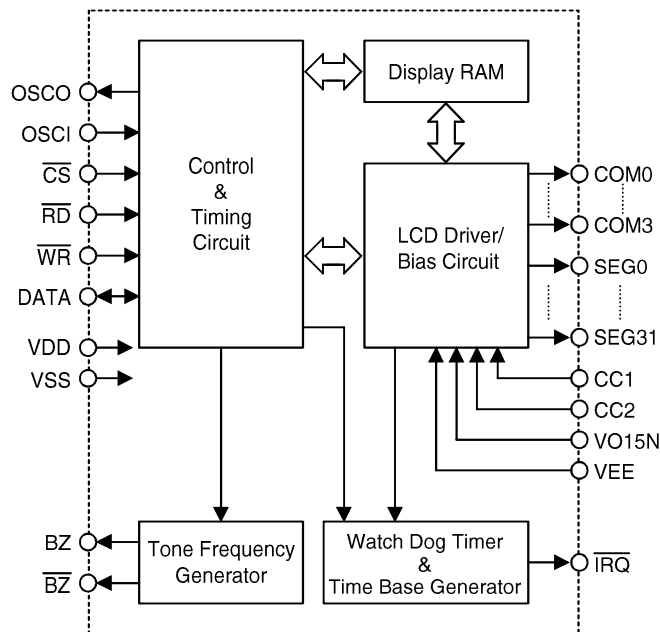
- Operating voltage: 2.4V~3.3V
- Low operating current <3μA at 3V
- External 32kHz crystal oscillator
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies (2K/4K)
- A built-in time base generator and a WDT
- Time base or WDT overflow output
- A 32×4 LCD driver
- A built-in 32×4 bit display RAM
- 3-wire serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- Three data accessing modes

General Description

The HT1620 is a 128 pattern, memory mapping, and multi-function LCD driver. The S/W configuration feature of the HT1620 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only

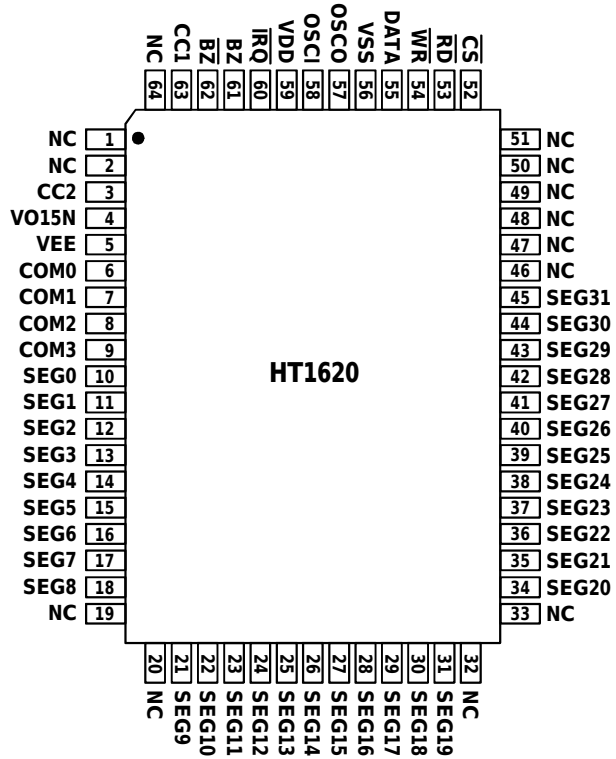
3 or 4 lines are required for the interface between the host controller and the HT1620. The HT162X series have many kinds of products that match various application.

Block Diagram

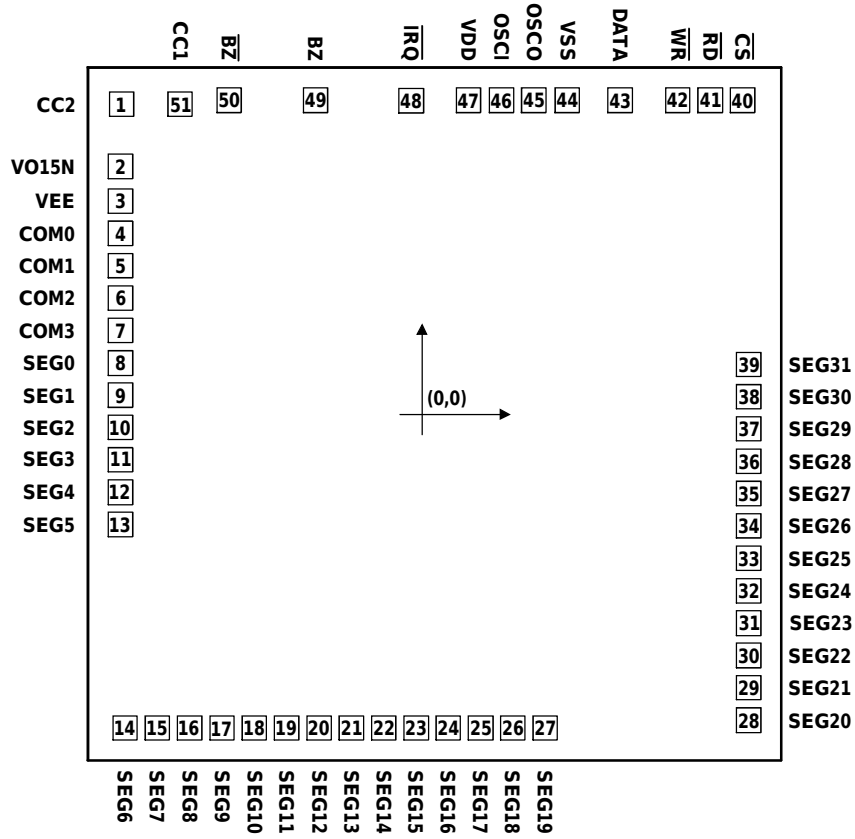


- Note: \overline{CS} : Chip selection
 BZ, \overline{BZ} : Tone outputs
 $\overline{WR}, \overline{RD}, DATA$: Serial interface
 $COM0\sim COM3, SEG0\sim SEG31$: LCD outputs
 \overline{IRQ} : Time base or WDT overflow output
 $VO15N$: Half voltage circuit output pin
 VEE : Double voltage circuit output pin
 $CC1/CC2$: External capacitor pin, for double voltage and half voltage circuit use

Pin Assignment (64 QFP)



Pad Assignment



Chip size: 142 × 141 (mil)²

* The IC substrate should be connected to VDD in the PCB layout artwork.

Pad Coordinates

Unit: mil

Pad No.	X	Y	Pad No.	X	Y
1	-61.58	63.62	27	25.29	-64.26
2	-61.83	50.83	28	66.98	-62.65
3	-61.83	43.73	29	66.98	-56.01
4	-61.83	37.10	30	66.98	-49.38
5	-61.83	30.47	31	66.98	-42.76
6	-61.83	23.84	32	66.98	-36.13
7	-61.83	17.21	33	66.98	-29.50
8	-61.83	10.58	34	66.98	-22.86
9	-61.83	3.95	35	66.98	-16.24
10	-61.83	-2.68	36	66.98	-9.60
11	-61.83	-9.31	37	66.98	-2.97
12	-61.83	-15.94	38	66.98	3.65
13	-61.83	-22.57	39	66.98	10.28
14	-60.90	-64.26	40	65.71	64.39
15	-54.27	-64.26	41	59.08	64.39
16	-47.64	-64.26	42	52.45	64.39
17	-41.01	-64.26	43	40.59	64.39
18	-34.38	-64.26	44	29.75	64.39
19	-27.75	-64.26	45	22.95	64.39
20	-21.12	-64.26	46	16.32	64.39
21	-14.49	-64.26	47	9.56	64.39
22	-7.86	-64.26	48	-2.21	64.30
23	-1.23	-64.26	49	-21.80	64.39
24	5.40	-64.26	50	-39.52	64.39
25	12.03	-64.26	51	-49.60	63.62
26	18.66	-64.26			

Pad Description

Pad No.	Pad Name	I/O	Function
40	\overline{CS}	I	Chip selection input with a pull-high resistor When the \overline{CS} is logic high, the data and command read from or written to the HT1620 are disabled. The serial interface circuit is also reset. But if the \overline{CS} is at a logic low level and is input to the \overline{CS} pad, the data and command transmission between the host controller and the HT1620 are all enabled.
41	\overline{RD}	I	READ clock input with a pull-high resistor Data in the RAM of the HT1620 are clocked out on the falling edge of the \overline{RD} signal. The clocked out data will appear on the DATA line. The host controller can use the next raising edge to latch the clocked out data.
42	\overline{WR}	I	WRITE clock input with a pull-high resistor Data on the DATA line are latched into the HT1620 on the rising edge of the \overline{WR} signal.
43	DATA	I/O	Serial data input/output with a pull-high resistor
44	VSS	I	Negative power supply, GND
45 46	OSCO OSCI	O I	The OSCI and OSCO pads are connected to a 32.768kHz crystal in order to generate a system clock.
47	VDD	I	Positive power supply
48	\overline{IRQ}	O	Time base or WDT overflow flag, NMOS open drain output
49, 50	BZ, \overline{BZ}	O	Tone frequency output pair (tristate output buffer)
51, 1	CC1, CC2	I	External capacitor pin, for double voltage and half voltage circuit use
2	VO15N	O	Half voltage circuit output pin
3	VEE	O	Double voltage circuit output pin
4~7	COM0~COM3	O	LCD common outputs
8~39	SEG0~SEG31	O	LCD segment outputs

Absolute Maximum Ratings

Supply Voltage	-0.3V~3.3V	Storage Temperature.....	-50°C~125°C
Input Voltage.....	VSS-0.3V~VDD+0.3V	Operating Temperature.....	-25°C~75°C

D.C. Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V _{DD}	Condition				
V _{DD}	Operating Voltage	—	—	2.4	—	3.3	V
I _{DD}	Operating Current	3V	No load*	—	2	3	μA
I _{STB}	Stand-by Current	3V	No load*	—	—	1	μA
V _{IL}	Input Low Voltage	3V	DATA, \overline{WR} , \overline{CS} , \overline{RD}	—	—	0.6	V
V _{IH}	Input High Voltage	3V	DATA, \overline{WR} , \overline{CS} , \overline{RD}	2.4	—	3.0	V
I _{OL1}	DATA, BZ, \overline{BZ} , \overline{IRQ}	3V	V _{OL} =0.3V	0.8	1.6	—	mA
I _{OH1}	DATA, BZ, \overline{BZ}	3V	V _{OH} =2.7V	-0.6	-1.2	—	mA
I _{OL2}	LCD Common Sink Current	3V	V _{OL} =0.3V	80	150	—	μA
I _{OH2}	LCD Common Source Current	3V	V _{OH} =2.7V	-70	-120	—	μA
I _{OL3}	LCD Segment Sink Current	3V	V _{OL} =0.3V	70	140	—	μA
I _{OH3}	LCD Segment Source Current	3V	V _{OH} =2.7V	-30	-60	—	μA
R _{PH}	Pull-High Resister	3V	DATA, \overline{WR} , \overline{CS} , \overline{RD}	40	80	150	kΩ

* No load: LCD OFF, Buzzer OFF, $\overline{CS}=\overline{WR}=\overline{RD}$ =High.

A.C. Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V _{DD}	Condition				
f _{SYS}	System Clock	3V	Crystal 32kHz	—	32	—	kHz
f _{LCD}	LCD Frame Frequency	—	Crystal 32kHz	—	64	—	Hz
	LCD Frame Frequency 1/2 Duty	—		—	64	—	Hz
	LCD Frame Frequency 1/3 Duty	—		—	56	—	Hz
	LCD Frame Frequency 1/4 Duty	—		—	64	—	Hz
t _{COM}	LCD Common Period	—	n: Number of COM	—	n/f _{LCD}	—	s
f _{CLK}	Serial Data Clock	3V	Write Mode	—	—	150	kHz
			Read Mode	—	—	75	kHz
f _{TONE}	Tone Frequency	—	—	—	2 or 4	—	kHz

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
tCS	Serial Interface Reset Pulse Width	—	\overline{CS}	—	250	—	ns
tw	Pulse Width Serial Data Clock (Figure 1)	3V	Write mode	3.34	—	—	μ s
			Read mode	6.67	—	—	μ s
trtf	Rise/Fall Time Serial Data Clock (Figure 1)	3V	—	—	120	—	ns
t _{su}	Setup Time DATA to Serial Data Clock (Figure 2)	3V	—	—	120	—	ns
t _h	Hold Time DATA to Serial Data Clock (Figure 3)	3V	—	—	120	—	ns
t _n	Low to \overline{CS} High Serial Data Clock (Figure 3)	3V	—	—	100	—	ns
t _{rec}	\overline{CS} High to Serial Data Clock High (Figure 3)	3V	—	—	100	—	ns
t _w	Serial Interface Reset High (Figure 3)	3V	—	—	250	—	ns
t _{su}	\overline{CS} Low to Serial Pulse Width Serial Data Clock High (Figure 3)	3V	—	—	100	—	ns

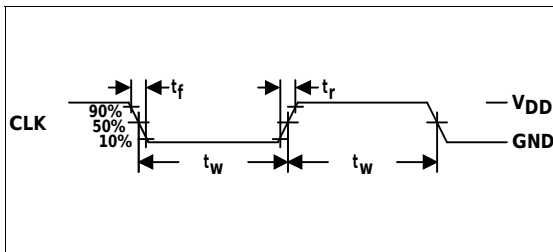


Figure 1.

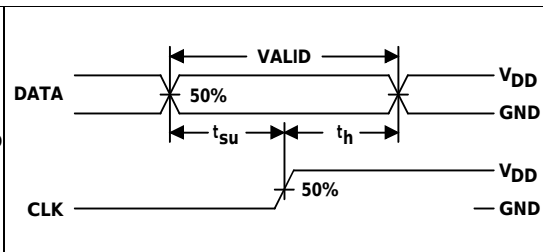


Figure 2.

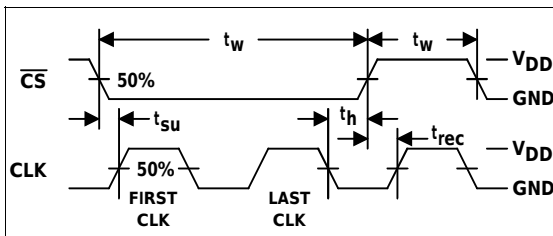
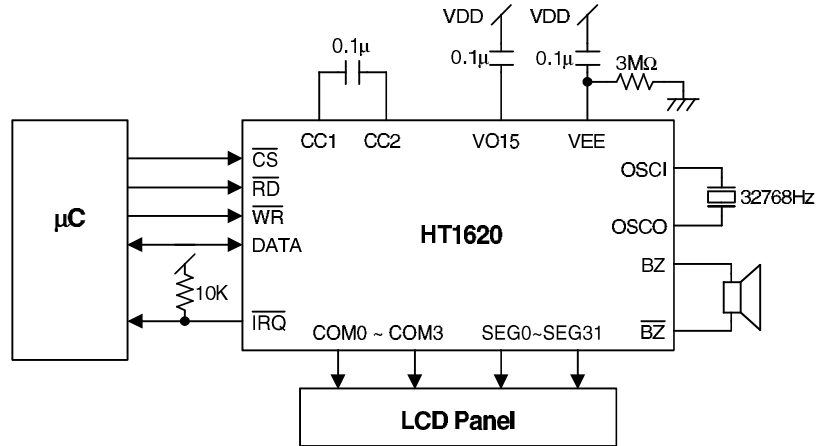


Figure 3.

Application Diagram



*: The connection of the \overline{IRQ} and \overline{RD} pin is selectable depending on the requirement of the host controller.

System Architecture

Display memory - RAM structure

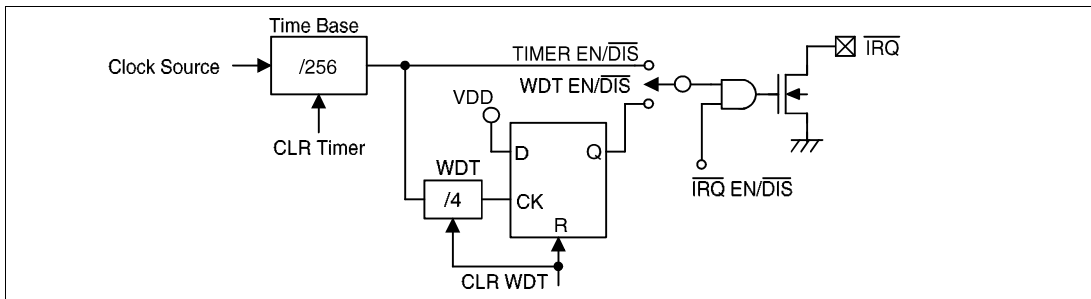
The static display RAM is organized into 32x4 bits and stores the display data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD patterns.

	COM3	COM2	COM1	COM0	
SEG0					0
SEG1					1
SEG2					2
SEG3					3
⋮					⋮
SEG31					31
	Bit 3	Bit 2	Bit 1	Bit 0	Addr Bit

RAM Mapping

Time base and watchdog timer (WDT)

The time base generator and WDT share the same divided (/256) counter. TIMER DIS/EN/CLR, WDT DIS/EN/CLR and IRQ/EN/DIS are independent from each other. Once the WDT time-out occurs, the $\overline{\text{IRQ}}$ pin will stay at a logic low level until the CLR WDT or the IRQ/DIS command is issued.



Timer and WDT Configurations

Buzzer tone output

A simple tone generator is implemented in the HT1622. The tone generator can output a pair of differential driving signals on the BZ and BZ/ which are used to generate a single tone.

LCD driver

The HT1620 is a 128 (32x4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HT1620 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz irrespective of being at a 32.768kHz crystal oscillator frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except the first command will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS & COM are the LCD panel related commands. Using the LCD related commands, the HT1620 can be compatible with most types of LCD panels.

Name	Command Code	Function
LCD OFF	1 0 0 0 0 0 0 0 0 1 0 X	Turn off LCD outputs
LCD ON	1 0 0 0 0 0 0 0 0 1 1 X	Turn on LCD outputs
BIAS & COM	1 0 0 0 0 1 0 a b X c X	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

Command format

The HT1620 can be configured by the S/W setting. There are two mode commands to configure the HT1620 resources and to transfer the LCD display data. The configuration mode of the HT1620 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

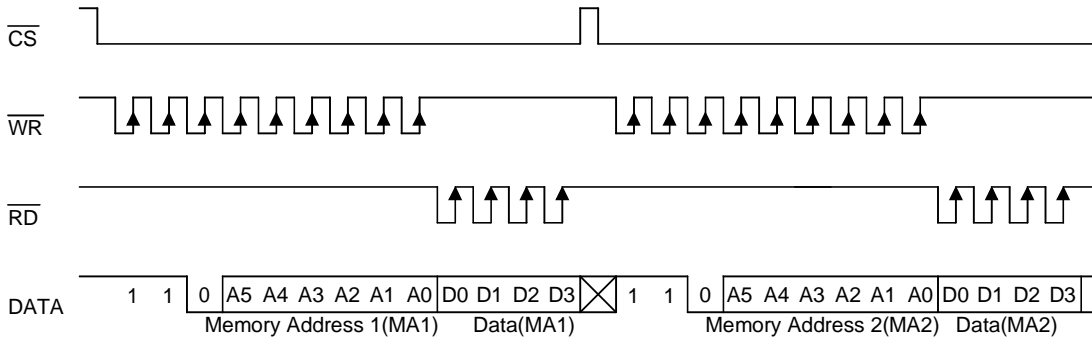
The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the \overline{CS} pin should be set to "1" and the previous operation mode will be reset also. Once the \overline{CS} pin returns to "0", a new operation mode ID should be issued first.

Interfacing

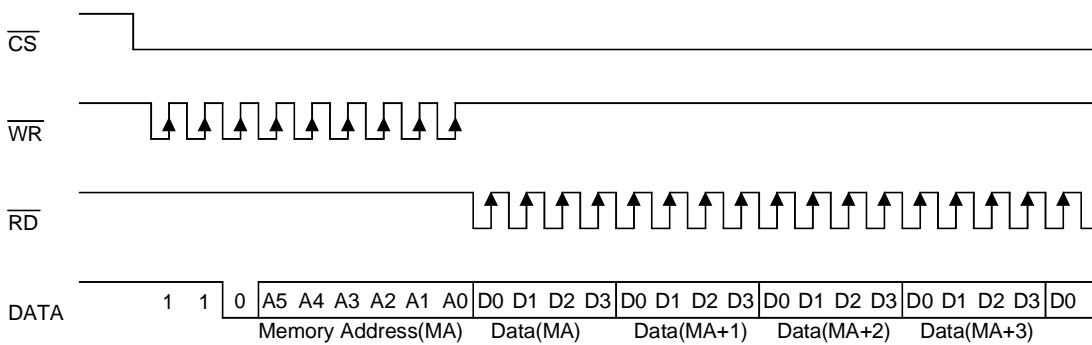
Only 4 lines are required to interface with the HT1620. The \overline{CS} line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1620. If the \overline{CS} pin is set to 1, the data and command issued between the host controller and the HT1620 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1620. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The \overline{RD} line is the READ clock input. Data in the RAM are clocked out on the falling edge of the \overline{RD} signal, and the clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the \overline{RD} signal. The \overline{WR} line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1620 on the rising edge of the \overline{WR} signal. There is an optional \overline{IRQ} line to be used as an interface between the host controller and the HT1620. The \overline{IRQ} pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the \overline{IRQ} pin of the HT1620.

Timing Diagrams

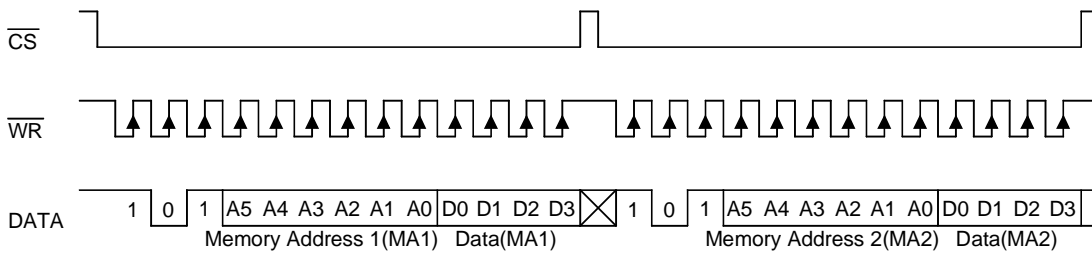
READ mode (command code: 1 1 0)



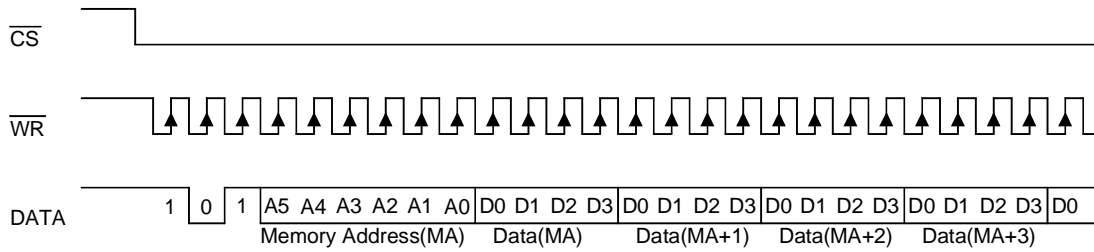
READ mode (successive address reading)



WRITE mode (command code: 1 0 1)

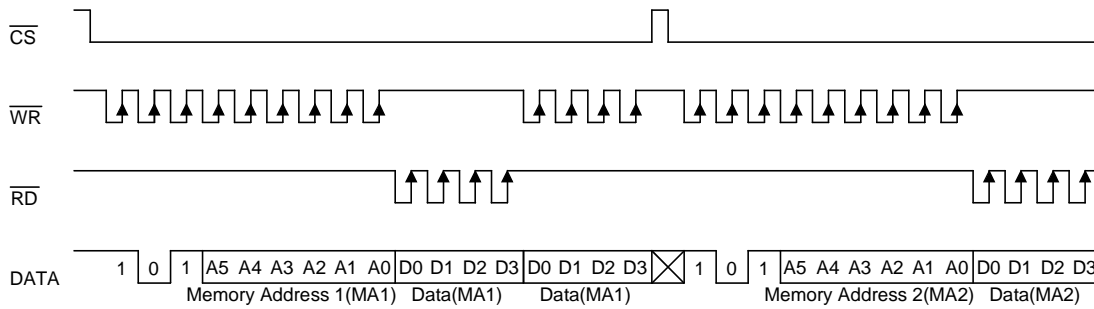


WRITE mode (successive address writing)

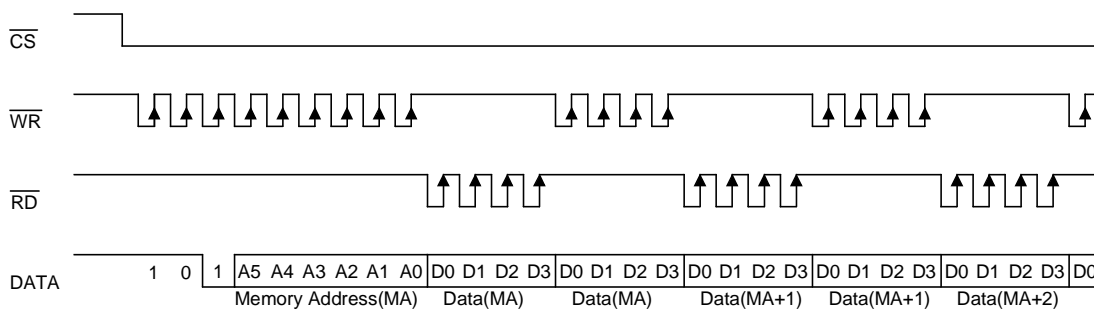


Note: It is suggested that the host controller should read in the data from the DATA line between the raising edge of the \overline{RD} line and the falling edge of the next \overline{RD} line.

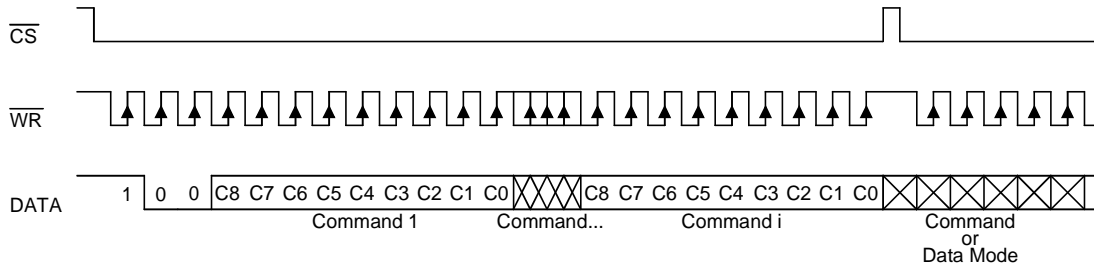
READ-MODIFY-WRITE mode (command code: 1 0 1)



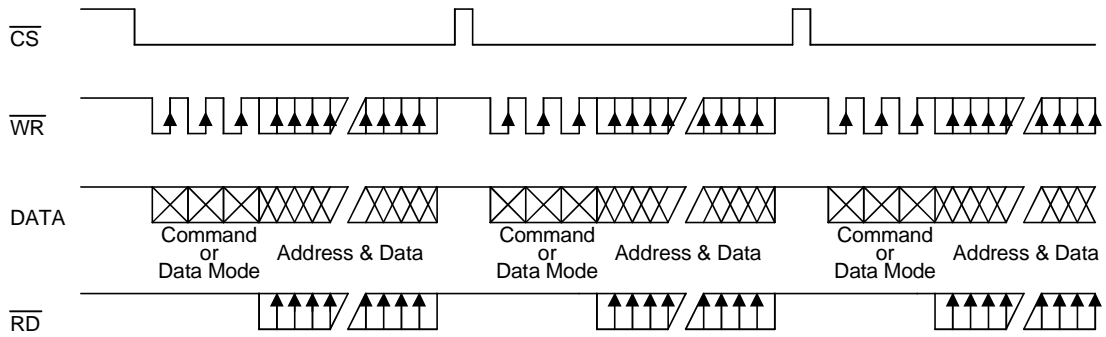
READ-MODIFY-WRITE mode (successive address accessing)



Command mode (command code: 1 0 0)



Mode (data & command mode)



Command Summarys

Name	Command Code	D/C	Function	Power On Reset Default
READ	1 1 0 a5 a4 a3 a2 a1 a0 d0 d1 d2 d3	D	Read data in the RAM	
WRITE	1 0 1 a5 a4 a3 a2 a1 a0 d0 d1 d2 d3	D	Write data to the RAM	
READ MODIFY WRITE	1 0 1 a5 a4 a3 a2 a1 a0 d0 d1 d2 d3	D	READ and WRITE to the RAM	
SYS DIS	1 0 0 0 0 0 0 0 0 0 0 X	C	Turn off both system oscillator and LCD bias generator	√
SYS EN	1 0 0 0 0 0 0 0 0 0 1 X	C	Turn on system oscillator	
LCD OFF	1 0 0 0 0 0 0 0 0 1 0 X	C	Turn off LCD bias generator	√
LCD ON	1 0 0 0 0 0 0 0 0 1 1 X	C	Turn on LCD bias generator	
TIMER DIS	1 0 0 0 0 0 0 0 1 0 0 X	C	Disable time base output	√
WDT DIS	1 0 0 0 0 0 0 0 1 0 1 X	C	Disable WDT time-out flag output	√
TIMER EN	1 0 0 0 0 0 0 0 1 1 0 X	C	Enable time base output	
WDT EN	1 0 0 0 0 0 0 0 1 1 1 X	C	Enable WDT time-out flag output	
TONE OFF	1 0 0 0 0 0 0 1 0 0 0 X	C	Turn off tone outputs	√
CLR TIMER	1 0 0 0 0 0 0 1 1 0 1 X	C	Clear the contents of time base generator	
CLR WDT	1 0 0 0 0 0 0 1 1 1 X X	C	Clear the contents of WDT stage	
BIAS 1/2	1 0 0 0 0 1 0 a b X 0 X	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
BIAS 1/3	1 0 0 0 0 1 0 a b X 1 X	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	1 0 0 0 1 0 X X X X X X	C	Tone frequency, 4kHz	
TONE 2K	1 0 0 0 1 1 0 X X X X X	C	Tone frequency, 2kHz	

Name	Command Code	D/C	Function	Power On Reset Default
$\overline{\text{IRQ}}$ DIS	1 0 0 1 0 0 X 0 X X X X	C	Disable $\overline{\text{IRQ}}$ output	√
$\overline{\text{IRQ}}$ EN	1 0 0 1 0 0 X 1 X X X X	C	Enable $\overline{\text{IRQ}}$ output	
F1	1 0 0 1 0 1 X 0 0 0 0 X	C	Time base clock output: 1Hz The WDT time-out flag after: 4s	
F2	1 0 0 1 0 1 X 0 0 0 1 X	C	Time base clock output: 2Hz The WDT time-out flage after: 2s	
F4	1 0 0 1 0 1 X 0 0 1 0 X	C	Time base clock output: 4Hz The WDT time-out flage after: 1s	
F8	1 0 0 1 0 1 X 0 0 1 1 X	C	Time base clock output: 8Hz The WDT time-out flage after: 1/2s	
F16	1 0 0 1 0 1 X 0 1 0 0 X	C	Time base clock output: 16Hz The WDT time-out flage after: 1/4s	
F32	1 0 0 1 0 1 X 0 1 0 1 X	C	Time base clock output: 32Hz The WDT time-out flage after: 1/8s	
F64	1 0 0 1 0 1 X 0 1 1 0 X	C	Time base clock output: 64Hz The WDT time-out flage after: 1/16s	
F128	1 0 0 1 0 1 X 0 1 1 1 X	C	Time base clock output: 128Hz The WDT time-out flage after:1/3 2s	√
TOPT	1 0 0 1 1 1 0 0 0 0 X	C	Test mode	
TNORMAL	1 0 0 1 1 1 0 0 0 1 X	C	Normal mode	√

Note: X : Don't care

a5~a0 : RAM addresses

d3~d0 : RAM data

D/C : Data/command mode

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from a 32.768kHz crystal oscillator. Calculation of the frequency is based on the system frequency sources as stated above. It is suggested that the host controller should initialize the HT1620 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1620.