

**LCD Product Line Selection Table**

	HT1620	HT1621	HT1622	HT16220	HT1623	HT1625	HT1626	HT1627	HT16270
<b>COM</b>	4	4	8	8	8	8	16	16	16
<b>SEG</b>	32	32	32	32	48	64	48	64	64
<b>Built-in Osc.</b>		√	√		√	√	√	√	
<b>Crystal Osc.</b>	√	√		√					√

### Features

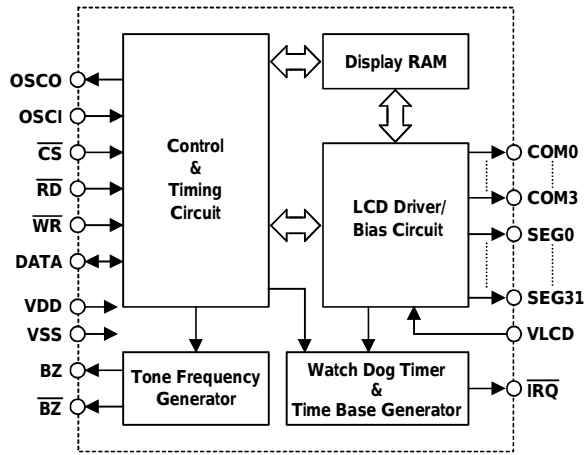
- Operating voltage : 2.4V~5.2V
- A built-in 256KHz RC oscillator
- External 32KHz crystal or 256KHz frequency source input
- Selection of 1/2 or 1/3 bias, and selection of 1/2 or 1/3 or 1/4 duty LCD applications
- Internal time base frequency sources
- Two selectable buzzer frequencies
- Power down command to reduce power consumption
- A built-in time base generator and a WDT
- Time base or WDT overflow output
- Eight time base/WDT clock sources
- A 32 × 4 LCD driver
- A built-in 32 × 4 bit display RAM
- Four-line serial interface
- Internal LCD driving frequency source
- Software configuration feature
- Data mode and command mode instructions
- Three data accessing modes
- Provide VLCD pin for adjusting LCD operating voltage

### General Description

The HT1621 is a 128 pattern, memory mapping, and multi-function LCD driver. The S/W configuration feature of the HT1621 makes it suitable for multiple LCD applications including LCD modules and display subsystems. Only

4 or 5 lines are required for the interface between the host controller and the HT1621. The HT1621 contains a power down command to reduce power consumption.

Block Diagram



Note:  $\overline{CS}$ : Chip selection  
 $\overline{BZ}$ ,  $\overline{BZ}$ : Tone outputs  
 $\overline{WR}$ ,  $\overline{RD}$ , DATA: Serial interface  
 COM0~COM3, SEG0~SEG31: LCD outputs  
 $\overline{IRQ}$ : Time base or WDT overflow output

Pin Assignment

SEG7	1	48	SEG8
SEG6	2	47	SEG9
SEG5	3	46	SEG10
SEG4	4	45	SEG11
SEG3	5	44	SEG12
SEG2	6	43	SEG13
SEG1	7	42	SEG14
SEG0	8	41	SEG15
$\overline{CS}$	9	40	SEG16
$\overline{RD}$	10	39	SEG17
$\overline{WR}$	11	38	SEG18
DATA	12	37	SEG19
VSS	13	36	SEG20
OSCO	14	35	SEG21
NC	15	34	SEG22
OSCI	16	33	SEG23
VDD/VLCD	17	32	SEG24
$\overline{IRQ}$	18	31	SEG25
BZ	19	30	SEG26
$\overline{BZ}$	20	29	SEG27
COM0	21	28	SEG28
COM1	22	27	SEG29
COM2	23	26	SEG30
COM3	24	25	SEG31

**HT1621**  
- 48 SSOP

SEG7	1	48	SEG8
SEG6	2	47	SEG9
SEG5	3	46	SEG10
SEG4	4	45	SEG11
SEG3	5	44	SEG12
SEG2	6	43	SEG13
SEG1	7	42	SEG14
SEG0	8	41	SEG15
$\overline{CS}$	9	40	SEG16
$\overline{RD}$	10	39	SEG17
$\overline{WR}$	11	38	SEG18
DATA	12	37	SEG19
VSS	13	36	SEG20
OSCO	14	35	SEG21
OSCI	15	34	SEG22
VLCD	16	33	SEG23
VDD	17	32	SEG24
$\overline{IRQ}$	18	31	SEG25
BZ	19	30	SEG26
$\overline{BZ}$	20	29	SEG27
COM0	21	28	SEG28
COM1	22	27	SEG29
COM2	23	26	SEG30
COM3	24	25	SEG31

**HT1621B**  
- 48 SSOP/PDIP

SEG5	1	28	SEG7
SEG3	2	27	SEG9
SEG1	3	26	SEG11
$\overline{CS}$	4	25	SEG13
$\overline{RD}$	5	24	SEG15
$\overline{WR}$	6	23	SEG17
DATA	7	22	SEG19
VSS	8	21	SEG21
VLCD	9	20	SEG23
VDD	10	19	SEG25
$\overline{IRQ}$	11	18	SEG27
BZ	12	17	SEG29
COM0	13	16	SEG31
COM1	14	15	COM2

**HT1621D**  
- 28 Skinny



**Pad Coordinates**

Unit: mil

Pad No.	X	Y	Pad No.	X	Y
1	-55.04	59.46	25	58.14	-25.29
2	-58.52	22.18	26	58.14	-18.66
3	-58.52	15.56	27	58.14	-11.94
4	-58.52	5.36	28	58.14	-5.31
5	-58.52	-4.51	29	58.14	1.32
6	-58.52	-11.14	30	58.14	7.95
7	-58.52	-34.76	31	58.14	14.58
8	-58.52	-41.90	32	58.14	21.21
9	-58.52	-49.13	33	55.55	59.46
10	-58.52	-59.08	34	48.92	59.46
11	-44.07	-59.08	35	42.29	59.46
12	-31.58	-59.08	36	35.66	59.46
13	-20.70	-59.08	37	29.03	59.46
14	-13.98	-59.08	38	22.40	59.46
15	-7.05	-59.08	39	15.77	59.46
16	-0.34	-59.08	40	9.14	59.46
17	6.33	-59.08	41	2.42	59.46
18	12.96	-59.08	42	-4.21	59.46
19	19.59	-59.08	43	-10.84	59.46
20	58.14	-58.44	44	-17.47	59.46
21	58.14	-51.81	45	-24.10	59.46
22	58.14	-45.18	46	-30.73	59.46
23	58.14	-38.55	47	-38.17	59.46
24	58.14	-31.92	48	-45.39	59.46

**Pad Description**

Pad No.	Pad Name	I/O	Function
1	$\overline{CS}$	I	Chip selection input with a pull-high resistor When the $\overline{CS}$ is logic high, the data and command read from or written to the HT1621 are disabled. The serial interface circuit is also reset. But if the $\overline{CS}$ is at a logic low level and is input to the $\overline{CS}$ pad, the data and command transmission between the host controller and the HT1621 are all enabled.
2	$\overline{RD}$	I	READ clock input with a pull-high resistor Data in the RAM of the HT1621 are clocked out on the falling edge of the $\overline{RD}$ signal. The clocked out data will appear on the DATA line. The host controller can use the next raising edge to latch the clocked out data.
3	$\overline{WR}$	I	WRITE clock input with a pull-high resistor Data on the DATA line are latched into the HT1621 on the rising edge of the $\overline{WR}$ signal.
4	DATA	I/O	Serial data input/output with a pull-high resistor

Pad No.	Pad Name	I/O	Function
5	VSS	I	Negative power supply, GND
7 6	OSCI OSCO	I O	The OSCI and OSCO pads are connected to a 32.768KHz crystal in order to generate a system clock. If the system clock comes from an external clock source, the external clock source should be connected to the OSCI pad. But if an on-chip RC oscillator is selected instead, the OSCI and OSCO pads can be left open.
8	VLCD	I	LCD power input
9	VDD	I	Positive power supply
10	$\overline{IRQ}$	O	Time base or WDT overflow flag, NMOS open drain output
11, 12	BZ, $\overline{BZ}$	O	Tone frequency output pair
13~16	COM0~COM3	O	LCD common outputs
48~17	SEG0~SEG31	O	LCD segment outputs

### Absolute Maximum Ratings\*

Supply Voltage ..... -0.3V~5.5V      Storage Temperature..... -50°C~125°C  
 Input Voltage.....VSS-0.3V~VDD+0.3V      Operating Temperature..... -25°C~75°C

\*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### D.C. Characteristics

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		VDD	Condition				
V <sub>DD</sub>	Operating Voltage	—	—	2.4	—	5.2	V
I <sub>DD</sub>	Operating Current	3V	No load	—	150	300	μA
		5V	On-chip RC oscillator	—	300	600	μA
I <sub>DD</sub>	Operating Current	3V	No load	—	60	120	μA
		5V	Crystal oscillator	—	120	240	μA
I <sub>DD</sub>	Operating Current	3V	No load	—	100	200	μA
		5V	External clock source	—	200	400	μA
I <sub>STB</sub>	Standby Current	3V	No load	—	0.1	5	μA
		5V	Power down mode	—	0.3	10	μA

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Condition				
V <sub>IL</sub>	Input Low Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	0	—	0.6	V
		5V		0	—	1.0	V
V <sub>IH</sub>	Input High Voltage	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	2.4	—	3.0	V
		5V		4.0	—	5.0	V
I <sub>OL1</sub>	DATA, BZ, $\overline{BZ}$ , $\overline{IRQ}$	3V	V <sub>OL</sub> =0.3V	0.5	1.2	—	mA
		5V	V <sub>OL</sub> =0.5V	1.3	2.6	—	mA
I <sub>OH1</sub>	DATA, BZ, $\overline{BZ}$	3V	V <sub>OH</sub> =2.7V	-0.4	-0.8	—	mA
		5V	V <sub>OH</sub> =4.5V	-0.9	-1.8	—	mA
I <sub>OL2</sub>	LCD Common Sink Current	3V	V <sub>OL</sub> =0.3V	80	150	—	μA
		5V	V <sub>OL</sub> =0.5V	150	250	—	μA
I <sub>OH2</sub>	LCD Common Source Current	3V	V <sub>OH</sub> =2.7V	-80	-120	—	μA
		5V	V <sub>OH</sub> =4.5V	-120	-200	—	μA
I <sub>OL3</sub>	LCD Segment Sink Current	3V	V <sub>OL</sub> =0.3V	60	120	—	μA
		5V	V <sub>OL</sub> =0.5V	120	200	—	μA
I <sub>OH3</sub>	LCD Segment Source Current	3V	V <sub>OH</sub> =2.7V	-40	-70	—	μA
		5V	V <sub>OH</sub> =4.5V	-70	-100	—	μA
R <sub>PH</sub>	Pull-High Resister	3V	DATA, $\overline{WR}$ , $\overline{CS}$ , $\overline{RD}$	40	80	150	kΩ
		5V		30	60	100	kΩ

### A.C. Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
f <sub>SYS1</sub>	System Clock	3V	On-chip RC oscillator	—	256	—	kHz
		5V		—	256	—	kHz
f <sub>SYS2</sub>	System Clock	3V	Crystal oscillator	—	32.768	—	kHz
		5V		—	32.768	—	kHz
f <sub>SYS3</sub>	System Clock	3V	External clock source	—	256	—	kHz
		5V		—	256	—	kHz
f <sub>LCD</sub>	LCD Clock	—	On-chip RC oscillator	—	f <sub>SYS1</sub> /1024	—	Hz
		—	Crystal oscillator	—	f <sub>SYS2</sub> /128	—	Hz
		—	External clock source	—	f <sub>SYS3</sub> /1024	—	Hz

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V <sub>DD</sub>	Conditions				
t <sub>COM</sub>	LCD Common Period	—	n: Number of COM	—	n/f <sub>LCD</sub>	—	s
f <sub>CLK1</sub>	Serial Data Clock ( $\overline{WR}$ pin)	3V	Duty cycle 50%	—	—	150	kHz
		5V		—	—	300	
f <sub>CLK2</sub>	Serial Data Clock ( $\overline{RD}$ pin)	3V	Duty cycle 50%	—	—	75	kHz
		5V		—	—	150	
f <sub>TONE</sub>	Tone Frequency	—	On-chip RC oscillator	—	2.0 or 4.0	—	kHz
t <sub>CS</sub>	Serial Interface Reset Pulse Width	—	$\overline{CS}$	—	250	—	ns
t <sub>w</sub>	Pulse Width Serial Data Clock (Figure 1)	3V	Write mode	3.34	—	—	μs
			Read mode	6.67			
		5V	Write mode	1.67			
			Read mode	3.34			
t <sub>trf</sub>	Rise/Fall Time Serial Data Clock (Figure 1)	3V	—	—	120	—	ns
		5V	—	—	120	—	
t <sub>su</sub>	Setup Time DATA to Serial Data Clock (Figure 2)	3V	—	—	120	—	ns
		5V	—	—	120	—	
t <sub>h</sub>	Hold Time DATA to Serial Data Clock (Figure 3)	3V	—	—	120	—	ns
		5V	—	—	120	—	
t <sub>n</sub>	Low to $\overline{CS}$ High Serial Data Clock (Figure 3)	3V	—	—	100	—	ns
		5V	—	—	100	—	
t <sub>rec</sub>	$\overline{CS}$ High to Serial Data Clock High (Figure 3)	3V	—	—	100	—	ns
		5V	—	—	100	—	
t <sub>w</sub>	Serial Interface Reset High (Figure 3)	3V	—	—	250	—	ns
		5V	—	—	250	—	
t <sub>su</sub>	$\overline{CS}$ Low to Serial Pulse Width Serial Data Clock High (Figure 3)	3V	—	—	100	—	ns
		5V	—	—	100	—	

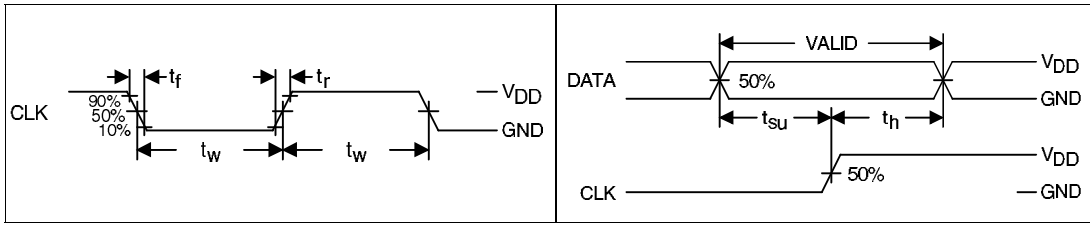


Figure 1.

Figure 2.

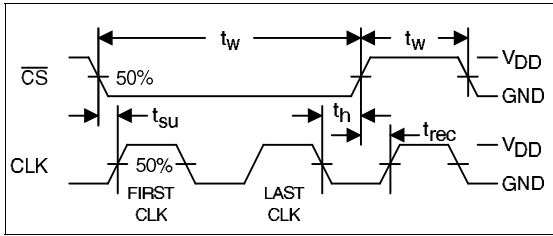
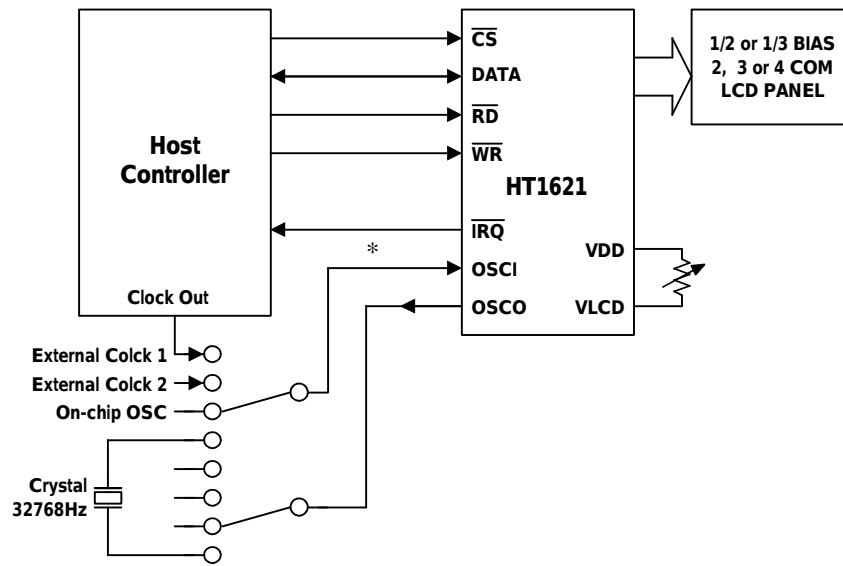


Figure 3.

### Application Diagram

Host controller with an HT1621 display system



\*: The connection of the  $\overline{\text{IRQ}}$  pin is selectable depending on the requirement of the host controller.

## System Architecture

### Display memory - RAM

The static display memory (RAM) is organized into 32x4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands. The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0	
SEG0					0
SEG1					1
SEG2					2
SEG3					3
...	...	...	...	...	...
SEG31					31
	Bit 3	Bit 2	Bit 1	Bit 0	Addr Bit

RAM Mapping

### System oscillator

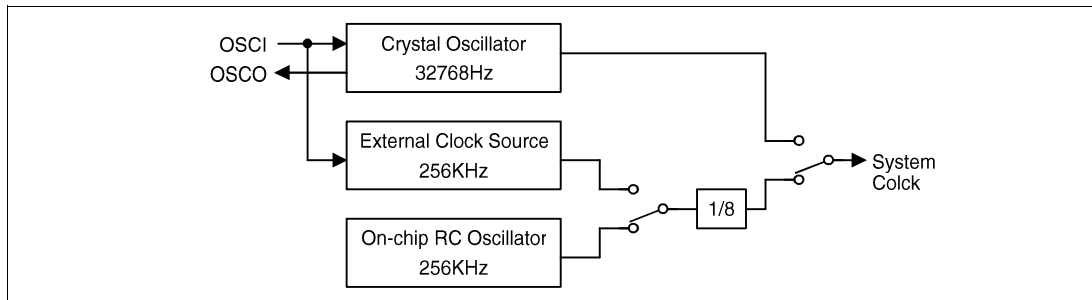
The HT1621 system clock is used to generate the time base/watch dog timer (WDT) clock frequency, LCD driving clock, and tone frequency. The source of the clock may be from an on-chip RC oscillator (256kHz), a crystal oscillator (32.768kHz), or an external 256kHz clock by the S/W setting. The configuration of the system

oscillator is as shown. After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off. That command is, however, available only for the on-chip RC oscillator or for the crystal oscillator. Once the system clock stops, the LCD display will become blank, and the time base/WDT lose its function as well.

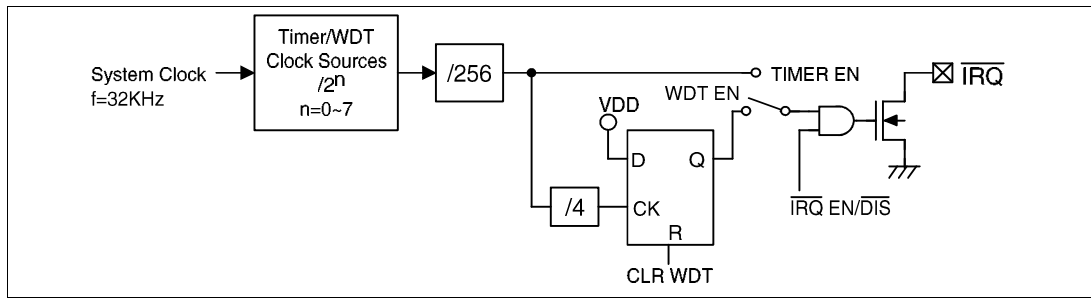
The LCD OFF command is used to turn the LCD bias generator off. After the LCD bias generator switches off by issuing the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a system power down command. But if the external clock source is chosen as the system clock, using the SYS DIS command can neither turn the oscillator off nor carry out the power down mode. The crystal oscillator option can be applied to connect an external frequency source of 32kHz to the OSCI pin. In this case, the system fails to enter the power down mode, similar to the case in the external 256kHz clock source operation. At the initial system power on, the HT1621 is at the SYS DIS state.

### Time base and watch dog timer (WDT)

The time base generator is comprised by an 8-stage count-up ripple counter and is designed to generate an accurate time base. The watch dog timer (WDT), on the other hand, is composed of an 8-stage time base generator along with a 2-stage count-up counter, and is designed to break the host controller or other subsystems from abnormal states such as unknown or unwanted jump, execution errors, etc. The WDT



System Oscillator Configuration



Timer and WDT Configurations

time-out will result in the setting of an internal WDT time-out flag. The outputs of the time base generator and of the WDT time-out flag can be connected to the  $\overline{\text{IRQ}}$  output by a command option. There are totally 8 frequency sources available for the time base generator and the WDT clock. The frequency is calculated by the following equation.

$$f_{\text{WDT}} = \frac{32\text{KHz}}{2^n}$$

where the value of n ranges from 0 to 7 by command options. The 32kHz in the above equation indicates that the source of the system frequency is derived from a crystal oscillator of 32.768kHz, an on-chip oscillator (256kHz), or an external frequency of 256kHz.

If an on-chip oscillator (256kHz) or an external 256kHz frequency is chosen as the source of the system frequency, the frequency source is by default prescaled to 32kHz by a 3-stage prescaler. Employing both the time base generator and the WDT related commands should be careful since the time base generator and WDT share the same 8-stage counter. For example, invoking the WDT DIS command disables the time base generator whereas executing the WDT EN command not only enables the time base generator but activates the WDT time-out flag output (connect the WDT time-out flag to the  $\overline{\text{IRQ}}$  pin). After the TIMER EN command is transferred, the WDT is disconnected from the  $\overline{\text{IRQ}}$  pin, and the output of the time base generator is connected to the  $\overline{\text{IRQ}}$  pin. The WDT can be cleared by executing the CLR WDT command, and the contents of the time base generator be cleared by executing the CLR WDT or the CLR TIMER command. The CLR WDT or the CLR TIMER command should be executed prior to

the WDT EN or the TIMER EN command respectively. Before executing the  $\overline{\text{IRQ}}$  EN command the CLR WDT or CLR TIMER command should be executed first. The CLR TIMER command has to be executed before switching from the WDT mode to the time base mode. Once the WDT time-out occurs, the  $\overline{\text{IRQ}}$  pin will stay at a logic low level until the CLR WDT or the  $\overline{\text{IRQ}}$  DIS command is issued. After the  $\overline{\text{IRQ}}$  output is disabled the  $\overline{\text{IRQ}}$  pin will stay at the floating state. The  $\overline{\text{IRQ}}$  output can be enabled or disabled by executing the  $\overline{\text{IRQ}}$  EN or the  $\overline{\text{IRQ}}$  DIS command, respectively. The  $\overline{\text{IRQ}}$  EN makes the output of the time base generator or of the WDT time-out flag appear on the  $\overline{\text{IRQ}}$  pin. The configuration of the time base generator along with the WDT are as shown. In the case of on-chip RC oscillator or of crystal oscillator, the power down mode can reduce power consumption since the oscillator can be turned on or off by the according system commands. At the power down mode the time base/WDT loses all its functions.

On the other hand, if an external clock is selected as the source of system frequency the SYS DIS command turns out invalid and the power down mode fails to be carried out. That is to say, after the external clock source is selected, the HT1621 will continue working until system power fails or the external clock source is removed. After the system power on, the  $\overline{\text{IRQ}}$  will be disabled.

**Tone output**

A simple tone generator is implemented in the HT1621. The tone generator can output a pair of differential driving signals on the BZ and  $\overline{\text{BZ}}$ , which are used to generate a single tone. By

Name	Command Code	Function
LCD OFF	<b>1 0 0 0 0 0 0 0 0 1 0 X</b>	Turn off LCD outputs
LCD ON	<b>1 0 0 0 0 0 0 0 0 1 1 X</b>	Turn on LCD outputs
BIAS & COM	<b>1 0 0 0 0 1 0 a b X c X</b>	c=0: 1/2 bias option c=1: 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option

executing the TONE4K and TONE2K commands there are two tone frequency outputs selectable. The TONE4K and TONE2K commands set the tone frequency to 4kHz and 2kHz, respectively. The tone output can be turned on or off by invoking the TONE ON or the TONE OFF command. The tone outputs, namely BZ and  $\overline{BZ}$ , are a pair of differential driving outputs used to drive a piezo buzzer. Once the system is disabled or the tone output is inhibited, the BZ and the  $\overline{BZ}$  outputs will stay at the low level.

#### LCD driver

The HT1621 is a 128 (32×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2 or 3 or 4 commons of LCD driver by the S/W configuration. This feature makes the HT1621 suitable for multiply LCD applications. The LCD driving clock is derived from the system clock. The value of the driving clock is always 256Hz irrespective of being at a 32.768kHz crystal oscillator frequency, an on-chip RC oscillator frequency, or an external frequency. The LCD corresponding commands are summarized in the table.

The bold form of 1 0 0, namely **1 0 0**, indicates the command mode ID. If successive commands have been issued, the command mode ID except the first command will be omitted. The LCD OFF command turns the LCD display off by disabling the LCD bias generator. The LCD ON command, on the other hand, turns the LCD display on by enabling the LCD bias generator. The BIAS & COM are the LCD panel related commands. Using the LCD related commands, the HT1621 can be compatible with most types of LCD panels.

#### Command format

The HT1621 can be configured by the S/W setting. There are two mode commands to configure the HT1621 resources and to transfer the LCD display data. The configuration mode of the HT1621 is called command mode, and its command mode ID is **1 0 0**. The command mode consists of a system configuration command, a system frequency selection command, an LCD configuration command, a tone frequency selection command, a timer/WDT setting command, and an operating command. The data mode, on the other hand, includes READ, WRITE, and READ-MODIFY-WRITE operations. The following are the data mode IDs and the command mode ID:

Operation	Mode	ID
READ	Data	1 1 0
WRITE	Data	1 0 1
READ-MODIFY-WRITE	Data	1 0 1
COMMAND	Command	1 0 0

The mode command should be issued before the data or command is transferred. If successive commands have been issued, the command mode ID, namely **1 0 0**, can be omitted. While the system is operating in the non-successive command or the non-successive address data mode, the  $\overline{CS}$  pin should be set to "1" and the previous operation mode will be reset also. Once the  $\overline{CS}$  pin returns to "0", a new operation mode ID should be issued first.

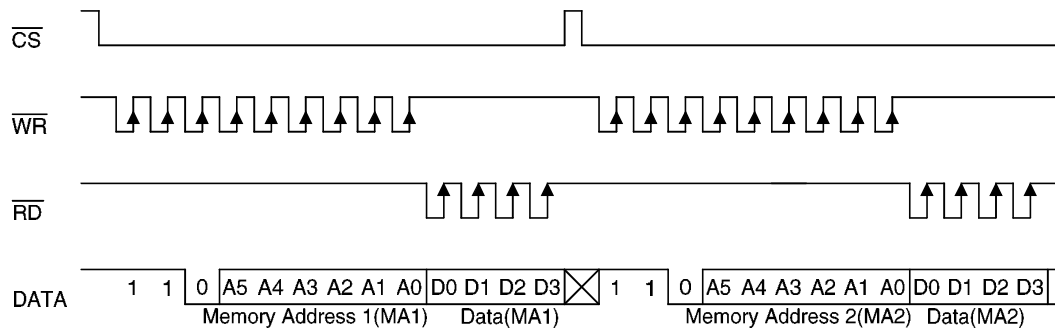
**Interfacing**

Only 4 lines are required to interface with the HT1621. The  $\overline{CS}$  line is used to initialize the serial interface circuit and to terminate the communication between the host controller and the HT1621. If the  $\overline{CS}$  pin is set to 1, the data and command issued between the host controller and the HT1621 are first disabled and then initialized. Before issuing a mode command or mode switching, a high level pulse is required to initialize the serial interface of the HT1621. The DATA line is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line. The  $\overline{RD}$  line is the READ clock input. Data in the RAM are clocked out on the falling edge of the  $\overline{RD}$  signal, and the

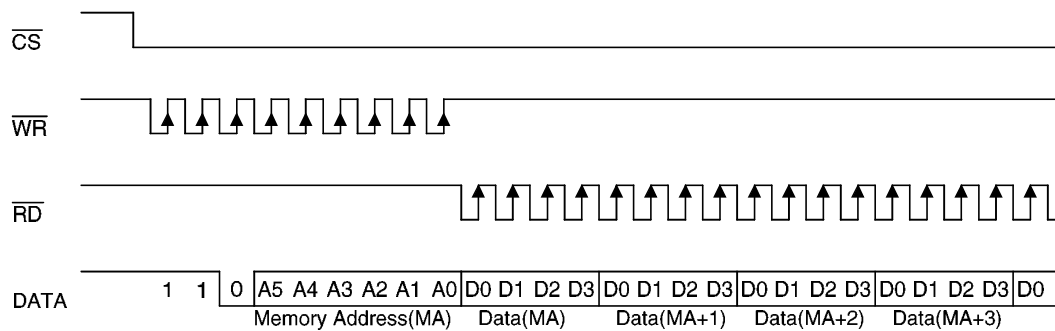
clocked out data will then appear on the DATA line. It is recommended that the host controller read in correct data during the interval between the rising edge and the next falling edge of the  $\overline{RD}$  signal. The  $\overline{WR}$  line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the HT1621 on the rising edge of the  $\overline{WR}$  signal. There is an optional  $\overline{IRQ}$  line to be used as an interface between the host controller and the HT1621. The  $\overline{IRQ}$  pin can be selected as a timer output or a WDT overflow flag output by the S/W setting. The host controller can perform the time base or the WDT function by being connected with the  $\overline{IRQ}$  pin of the HT1621.

**Timing Diagrams**

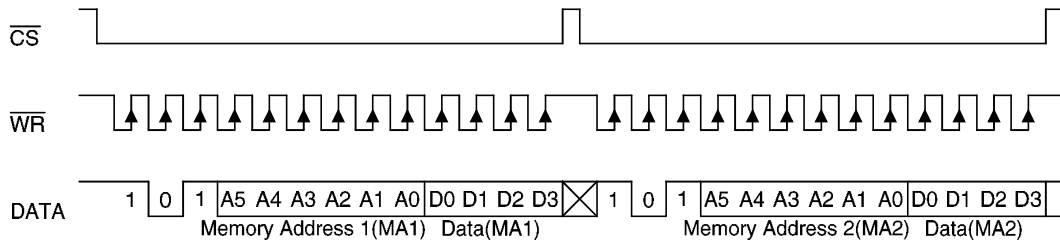
**READ mode (command code : 1 1 0)**



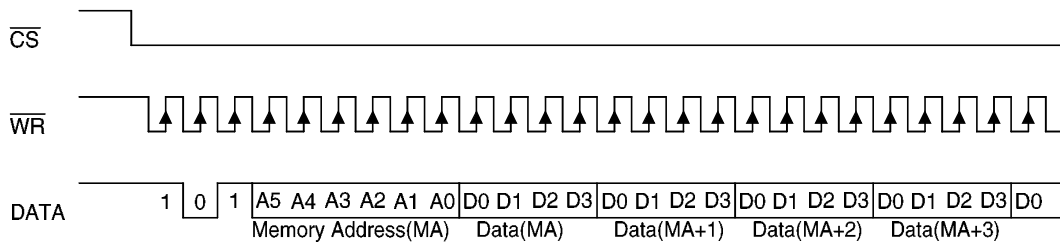
**READ mode (successive address reading)**



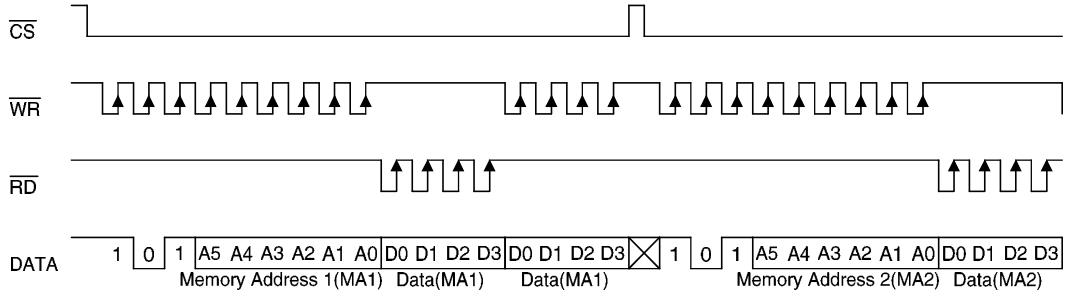
**WRITE mode (command code : 1 0 1)**



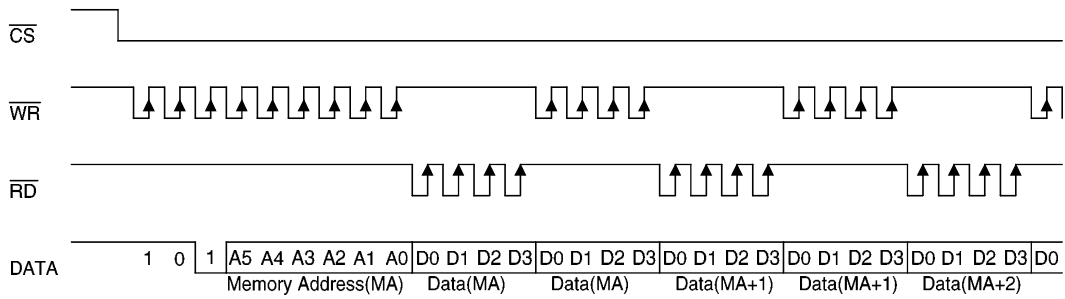
**WRITE mode(successive address writing)**



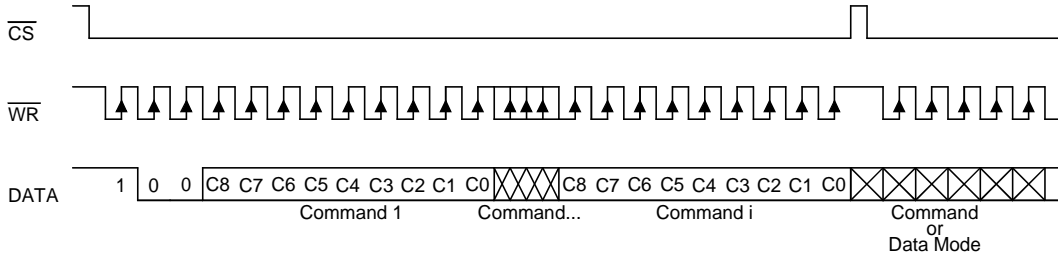
**READ-MODIFY-WRITE mode (command code : 1 0 1)**



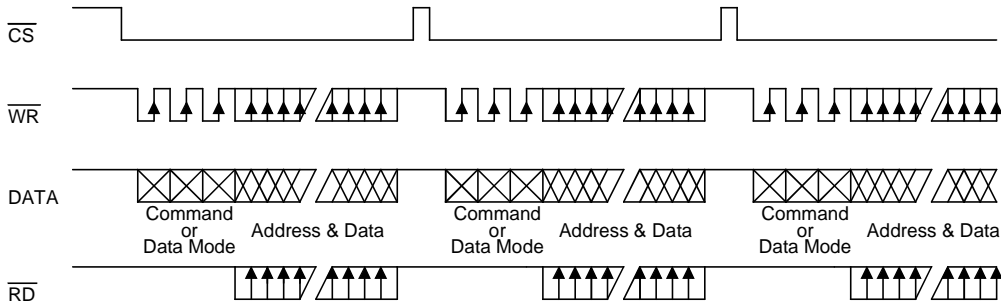
**READ-MODIFY-WRITE mode(successive address accessing)**



**Command mode (command code : 1 0 0)**



**Mode (data & command mode)**



**Note:** It is suggested that the host controller should read in the data from the DATA line between the raising edge of the RD line and the falling edge of the next RD line.

## Command Summary

Name	Command Code	D/C	Function	Power On Reset Default
READ	<b>1 1 0</b> a5 a4 a3 a2 a1 a0 d0 d1 d2 d3	D	Read data in the RAM	
WRITE	<b>1 0 1</b> a5 a4 a3 a2 a1 a0 d0 d1 d2 d3	D	Write data to the RAM	
READ MODIFY WRITE	<b>1 0 1</b> a5 a4 a3 a2 a1 a0 d0 d1 d2 d3	D	READ and WRITE to the RAM	
SYS DIS	<b>1 0 0 0 0 0 0 0 0 0 0 X</b>	C	Turn off both system oscillator and LCD bias generator	√
SYS EN	<b>1 0 0 0 0 0 0 0 0 0 1 X</b>	C	Turn on system oscillator	
LCD OFF	<b>1 0 0 0 0 0 0 0 0 1 0 X</b>	C	Turn off LCD bias generator	√
LCD ON	<b>1 0 0 0 0 0 0 0 0 1 1 X</b>	C	Turn on LCD bias generator	
TIMER DIS	<b>1 0 0 0 0 0 0 0 1 0 0 X</b>	C	Disable time base output	
WDT DIS	<b>1 0 0 0 0 0 0 0 1 0 1 X</b>	C	Disable WDT time-out flag output	
TIMER EN	<b>1 0 0 0 0 0 0 0 1 1 0 X</b>	C	Enable time base output	
WDT EN	<b>1 0 0 0 0 0 0 0 1 1 1 X</b>	C	Enable WDT time-out flag output	
TONE OFF	<b>1 0 0 0 0 0 0 1 0 0 0 X</b>	C	Turn off tone outputs	√
TONE ON	<b>1 0 0 0 0 0 0 1 0 0 1 X</b>	C	Turn on tone outputs	
CLR TIMER	<b>1 0 0 0 0 0 0 1 1 X X X</b>	C	Clear the contents of time base generator	
CLR WDT	<b>1 0 0 0 0 0 0 1 1 1 X X</b>	C	Clear the contents of WDT stage	
XTAL 32K	<b>1 0 0 0 0 0 1 0 1 X X X</b>	C	System clock source, crystal oscillator	
RC 256K	<b>1 0 0 0 0 0 1 1 0 X X X</b>	C	System clock source, on-chip RC oscillator	√
EXT 256K	<b>1 0 0 0 0 0 1 1 1 X X X</b>	C	System clock source, external clock source	
BIAS 1/2	<b>1 0 0 0 0 1 0 a b X 0 X</b>	C	LCD 1/2 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	

Name	Command Code	D/C	Function	Power On Reset Default
BIAS 1/3	<b>1 0 0 0 0 1 0 a b X 1 X</b>	C	LCD 1/3 bias option ab=00: 2 commons option ab=01: 3 commons option ab=10: 4 commons option	
TONE 4K	<b>1 0 0 0 1 0 X X X X X X</b>	C	Tone frequency, 4kHz	
TONE 2K	<b>1 0 0 0 1 1 X X X X X X</b>	C	Tone frequency, 2kHz	
$\overline{\text{IRQ}}$ DIS	<b>1 0 0 1 0 0 X 0 X X X X</b>	C	Disable $\overline{\text{IRQ}}$ output	√
$\overline{\text{IRQ}}$ EN	<b>1 0 0 1 0 0 X 1 X X X X</b>	C	Enable $\overline{\text{IRQ}}$ output	
F1	<b>1 0 0 1 0 1 X X 0 0 0 X</b>	C	Time base/WDT clock output 1Hz	
F2	<b>1 0 0 1 0 1 X X 0 0 1 X</b>	C	Time base/WDT clock output 2Hz	
F4	<b>1 0 0 1 0 1 X X 0 1 0 X</b>	C	Time base/WDT clock output 4Hz	
F8	<b>1 0 0 1 0 1 X X 0 1 1 X</b>	C	Time base/WDT clock output 8Hz	
F16	<b>1 0 0 1 0 1 X X 1 0 0 X</b>	C	Time base/WDT clock output 16Hz	
F32	<b>1 0 0 1 0 1 X X 1 0 1 X</b>	C	Time base/WDT clock output 32Hz	
F64	<b>1 0 0 1 0 1 X X 1 1 0 X</b>	C	Time base/WDT clock output 64Hz	
F128	<b>1 0 0 1 0 1 X X 1 1 1 X</b>	C	Time base/WDT clock output 128Hz	√
TOPT	<b>1 0 0 1 1 1 0 0 0 0 0 X</b>	C	Test mode	
TNORMAL	<b>1 0 0 1 1 1 0 0 0 1 1 X</b>	C	Normal mode	√

Note:

X : Don't care

a5~a0 : RAM addresses

d3~d0 : RAM data

D/C : Data/command mode

All the bold forms, namely **1 1 0**, **1 0 1**, and **1 0 0**, are mode commands. Of these, **1 0 0** indicates the command mode ID. If successive commands have been issued, the command mode ID except the first command will be omitted. The source of the tone frequency and of the time base/WDT clock frequency can be derived from an on-chip 256kHz RC oscillator, a 32.768kHz crystal oscillator, or an external 256kHz clock. Calculation of the frequency is based on the system frequency sources as stated above. It is suggested that the host controller should initialize the HT1621 after power on reset, for power on reset may fail, which in turn leads to the malfunctioning of the HT1621.